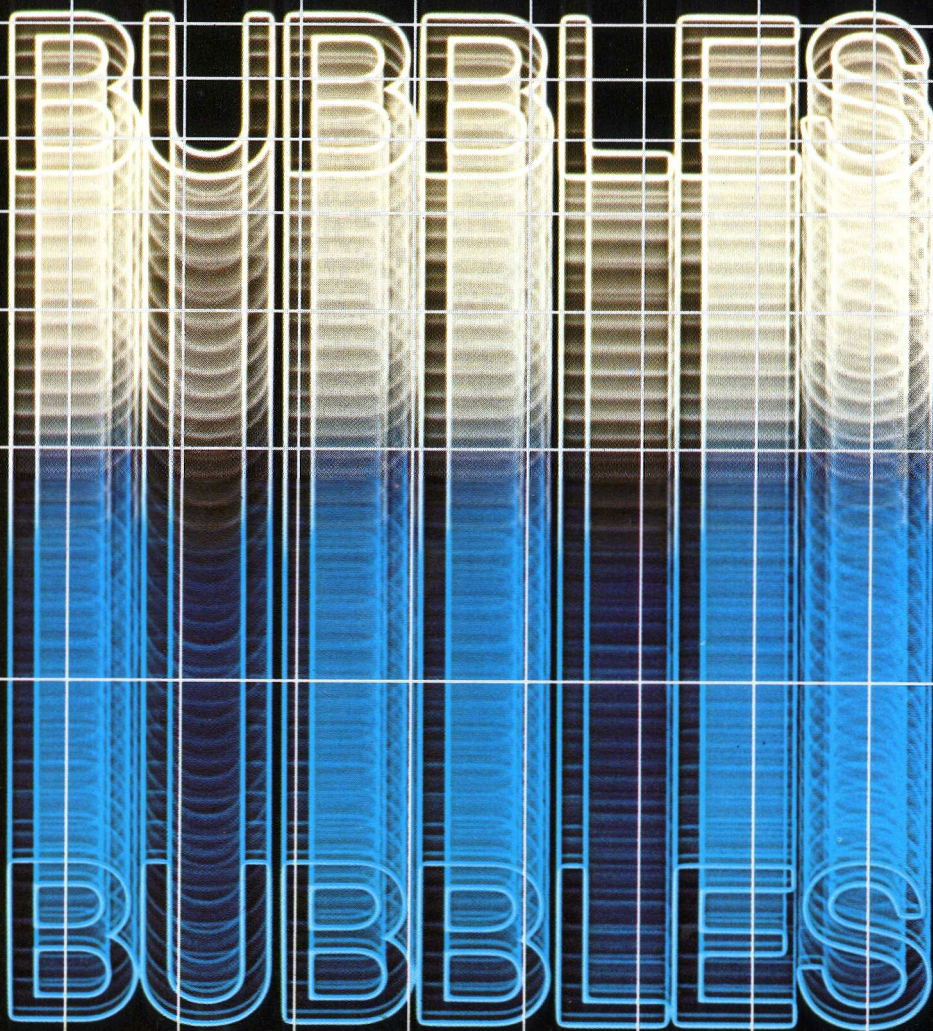


intel®

Magnetic Bubble Storage Data Catalog

February 1981





**BUBBLE STORAGE
DATA CATALOG**

FEBRUARY 1981

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INTRODUCTION

Welcome to the Intel Bubble Memory Storage Data Catalog where you'll find the data sheets you need to start implementing your own Intel bubble memory storage system.

Intel brings you all the key components, development kits and assembled bubble memory boards required for a total solution to your non-volatile mass storage requirements.

With bubble storage from Intel, your system gains the advantages of improved reliability and ruggedness, reduced size, weight and power requirements, and significant reductions in system maintenance.

HERE'S HOW TO USE INTEL® BUBBLE MEMORY IN A PRODUCTION ENVIRONMENT

Component Kits

Intel makes it easy for you to get into production, with BPK70 1-Megabit Bubble Storage Sub-Systems. Each BPK70 kit provides all the key components your board will require for one million bits of bubble storage. Kits consist of:

- 7110 1-Megabit Bubble Memory
- 7230 Current Pulse Generator
- 7242 Dual Formatter/Sense Amplifier
- 7250 Coil Pre-Driver
- Two 7254 Quad VMOS Drive Transistors
- 7904 Socket for 7110 Memory

BPK70 storage sub-systems operate under the direction of an Intel 7220COMP Bubble Memory Controller. Each 7220COMP Controller handles up to eight megabits of storage. Larger systems may be constructed using additional BPK70 kits and the appropriate number of 7220COMP Controllers.

7220COMP Controller

Bubble Memory Boards

Intel iSBC 254 Bubble Memory Boards are completely assembled and tested single-board bubble storage systems. They are designed for use with microprocessor-based systems and include an interface to Multibus™ systems.

If you are already an Intel OEM customer using the Multibus system and the iRMX™ Operating System software, iSBC 254 board compatibility allows you to substantially reduce product development cycles. You can concentrate on the application at hand to realize the competitive advantages of getting your product quickly to market.

The Intel iSBC 254 boards contain the Intel 7220 Bubble Memory Controller and one, two, or four 7110 1-Megabit Bubble Memories:

- iSBC 254-1 (128K Bytes)
- iSBC 254-2 (256K Bytes)
- iSBC 254-4 (512K Bytes)

HERE'S WHAT YOU WILL REQUIRE FOR PROTOTYPING AND EVALUATION

Component Kits

Intel BPK72 Bubble Storage Prototype Kits are designed to help you get started quickly into bubble memory design. They provide all the key components you require to prototype a 1-megabit bubble storage system for your microprocessor-based system. The kit is easily assembled and interfaced to your own microprocessor system.

BPK72 Kits consist of:

- BPK70 1-Megabit Bubble Storage Sub-System kit
- 7220BRD Controller (Fully assembled 7220COMP Controller)
- Blank 10 cm x 10 cm board
- BPK72 User's Manual and accessories

Bubble Memory Boards

Intel iSBC 254 Bubble Memory Boards are ideal for the rapid prototyping of Multibus storage systems. With the use of an Intel INTELLEC™ Microcomputer Development System, and an iSBC 254 bubble memory board, it is possible to quickly construct a bubble memory demonstration system.

iSBC 254 boards contain the Intel 7220 Bubble Memory Controller and one, two, or four 7110 1-Megabit Bubble Memories.

HERE'S THE SOFTWARE YOU'LL NEED

The BPK70 Bubble Storage Sub-Systems and BPK72 Bubble Storage Prototype Kits are supported by Intel's BMDS software package, or by your own user-written programs.

Software drivers are available for the iRMX/80 and iRMX 86 as operating systems to support the iSBC 254 board. TEST-254, a set of programs which diagnose the iSBC 254 and which can be used to demonstrate the functions of the board, is available for use with the Intel INTELLEC Microprocessor Development System. This is especially useful when writing your own software to support the iSBC 254 board.

HOW TO ORDER BUBBLE MEMORY STORAGE SYSTEMS AND KITS

Today, Intel can provide you with the kits, boards and software you will require to gain the many advantages of bubble memory systems.

For additional information, or to place an order, pick up your telephone and talk to your local Intel distributor or Intel Sales Office. The telephone numbers are located at the back of this Data Catalog. Let these Intel people help you find the most cost-effective ways to implement your bubble storage systems.

In ordering, remember that the BPK72 Bubble Storage Prototype Kits give you manuals and extra accessories to get you started into bubble memories. When you want to go into production with your own boards, you only need to buy the BPK70 1-Megabit Bubble Storage Sub-Systems with the appropriate number of 7220COMP Controllers.

BPK70 1-Megabit Bubble Storage Sub-Systems (Production Kits)

Part Number	Temperature Range
BPK70-0	0-50°C
BPK70-1	0-70°C
BPK70-2	10-50°C

7220COMP Controller (Components for customer board)

Part Number	Temperature Range
7220COMP	0-70°C

BPK72 Bubble Storage Prototype Kit

Part Number	Temperature Range
BPK72-0	0-50°C
BPK72-1	0-70°C
BPK72-2	10-50°C

7220BRD Controller (Assembled Board)

Part Number	Temperature Range
7220BRD	0-70°C

iSBC 254 Bubble Memory Boards

Part Number	Memory Size	Temperature Range
iSBC 254-1A	128K Bytes	0–55°C
iSBC 254-1B	128K Bytes	0–40°C
iSBC 254-2A	256K Bytes	0–55°C
iSBC 254-2B	256K Bytes	0–40°C
iSBC 254-4A	512K Bytes	0–55°C
iSBC 254-4B	512K Bytes	0–40°C

Software

BMDS Extended Monitor Software for BPK70 and BPK72 Kits is available from Intel INSITE™ Library.

TEST-254 hardware diagnostics used with iSBC 254 boards and Intel INTELLEC Microprocessor Development System, is available with the iSBC 254 board.

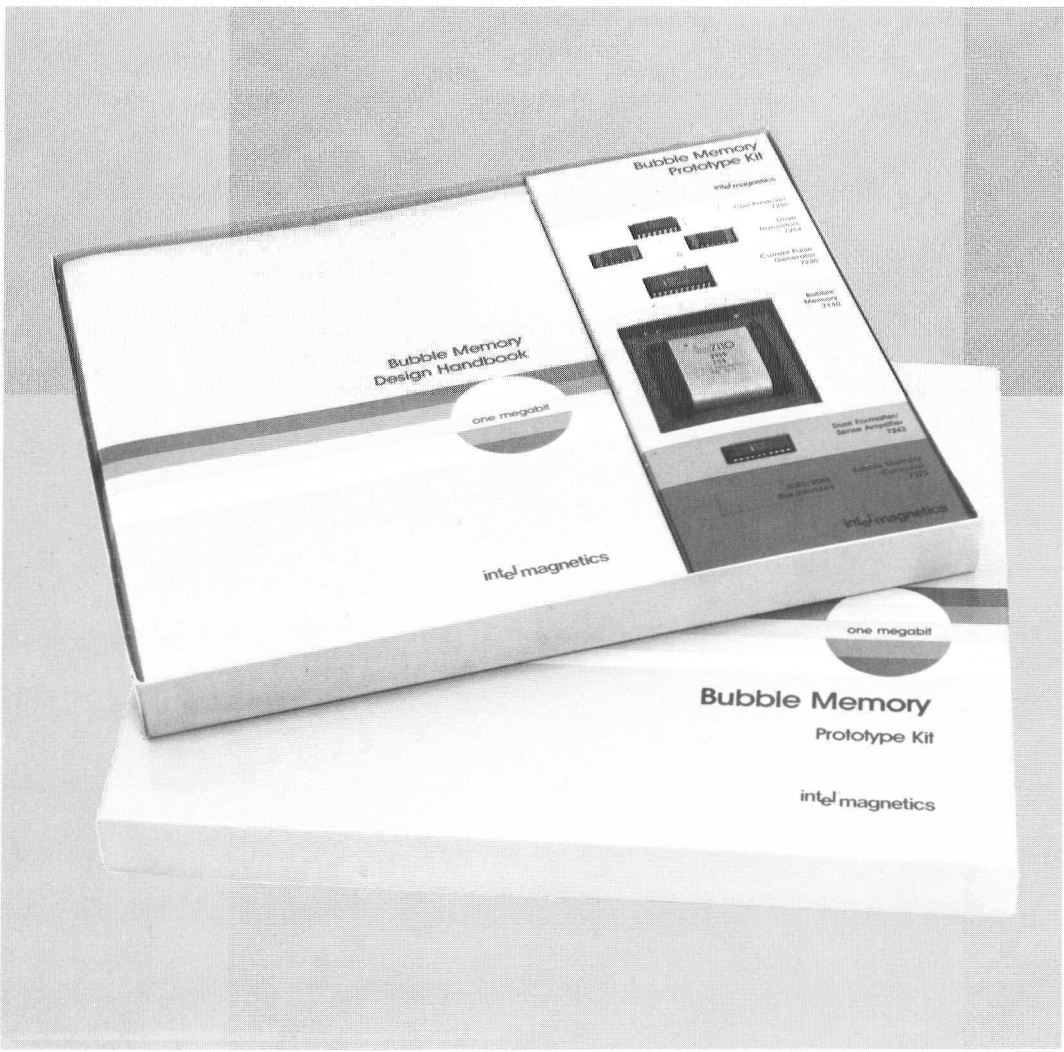
Drivers for iRMX/80 and iRMX 86 Operating Systems support of the iSBC 254 board are available from Intel INSITE Library in single- and double-density diskettes.



BPK72 BUBBLE STORAGE PROTOTYPE KIT

- One BPK70 1 Megabit Bubble Storage Subsystem
- One 7220BRD Controller
- Blank 10 cm x 10 cm PC Board for Assembly
- Complete with Accessories and Documentation for Prototyping

BPK72 prototype kit contains the necessary components, accessories and documentation required to build a 1 megabit bubble storage prototype system with minimum design effort. Application information on system interconnections is included.



ORDERING INFORMATION

Order Code	Description
BPK72-0	0-50°C 1 Megabit Storage System Prototype Kit
BPK72-1	0-70°C 1 Megabit Storage System Prototype Kit
BPK72-2	10-50°C 1 Megabit Storage System Prototype Kit

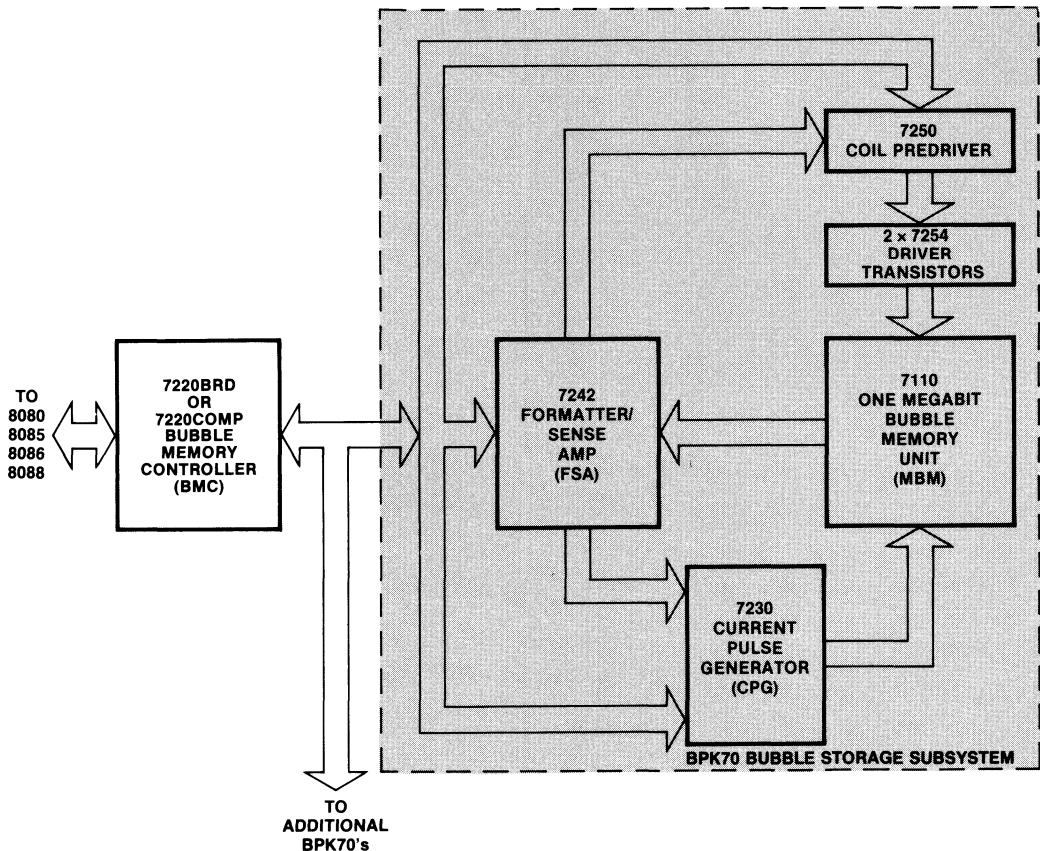
ITEMS IN KIT

Item	Part/Manual Number
BPK72 User's Manual	121685
Blank Printed Circuit Board	IMB-72
Socket for 7110	7904
Seed Module	7901
VMOS Transistor	7902
Solder Tip	7903
Dummy Module	7900
7220 BRD	Bubble Memory Controller
7230	Current Pulse Generator
7242	Dual Formatter/Sense Amp
7250	Coil Pre-Driver
2 x 7254	Quad VMOS Drive Transistors



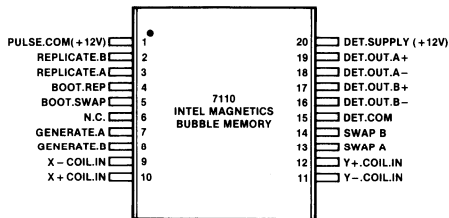
BPK70 1 MBit BUBBLE STORAGE SUBSYSTEM

- Contains Components for Production of 1 MBit Bubble Storage Subsystem
- One 7230 Current Pulse Generator
- One 7242 Dual Formatter/Sense Amplifier
- One 7250 Coil Pre-Driver
- Two 7254 Quad VMOS Drive Transistors
- One 7110 1 MBit Bubble Memory
- One 7904 Socket for 7110



ORDER INFORMATION

Part Number	Description
BPK70-0	0-50°C 1 MBit Bubble Storage Sub-System
BPK70-1	0-70°C 1 MBit Bubble Storage Sub-System
BPK70-2	10-50°C 1 MBit Bubble Storage Sub-System



NOTE THAT PINS 13 AND 14 SHOULD BE EXTERNALLY CONNECTED.

PIN CONFIGURATION

GENERAL FUNCTIONAL DESCRIPTION

The Intel Magnetics 7110 is a 1 megabit bubble memory module organized as two identical 512K binary half sections. See Major Track-Minor Loop architecture diagram. Each half section is in turn organized as two 256K subsections referred to as *quads*.

The module consists of a bubble die mounted in a substrate that accommodates two orthogonal drive coils that surround the die. The drive coils produce a rotating magnetic field in the plane of the die when they are excited by 90° phase shifted triangular current waveforms. The rotating in-plane field is responsible for bubble propagation. One drive field rotation propagates all bubbles in the device one storage location (or cycle). The die-substrate-coil sub-assembly is enclosed in a package consisting of permanent magnets and a shield. The shield serves as a flux return path for the permanent magnets in addition to isolating the device from stray magnetic fields. The permanent magnets produce a bias field that is nearly perpendicular to the plane of the die. This field supports the existence of the bubble domains.

The package is constructed to maintain a 2.5 degree tilt between the plane of the bias magnet faces and the plane of the die. This serves to introduce a small component of the bias field into the plane of the die. During operation when the drive coils are energized this small in-plane component is negligible. During standby or when power is removed the small inplane field ensures that the bubbles will be confined to their appropriate storage locations. The direction of the in-plane field introduced by the package tilt (holding field) is coincident with the 0° phase direction of the drive field.

Quad Architecture

A 7110 quad sub-section is composed of the following elements shown on the architecture diagram.

1) Storage Loops

Eighty identical 4096 bit storage loops provide a total maximum capacity of 327,680 bits. The excess storage is provided for two purposes: a) it allows a redundancy scheme to increase device yield; and b) it provides the extra storage required to implement error correction.

2) Replicating Generator (GEN)

The generator operates by replicating a seed bubble that is always present at the generator site, (GEN).

3) Input Track and Swap Gate

Bubbles following generation are propagated down an input track. Bubbles are transferred to/from the input track from/to the 80 storage loops via series connected swap gates spaced every four propagation cycles along the track. The swap gate's ability to transfer bubbles in both directions during an operation eliminates the overhead associated with removing old data from the loops before new data can be written. The swap gate is designed to function such that the logical storage loop position occupied by the bubble transferred out of each loop is filled by the bubble being transferred into each loop. Transferred out bubbles propagate down the remaining portion of the input track where they are dumped into a bubble bucket guard rail.

4) Output Track and Replicate Gate

Bubbles are read out of the storage loops in a non-destructive fashion via a set of replicate gates. The bubble is split in two. The leading bubble is retained in the storage loop and the trailing bubble is transferred onto the output track. Replicate gates are spaced every four propagation cycles along the output track.

5) Detector

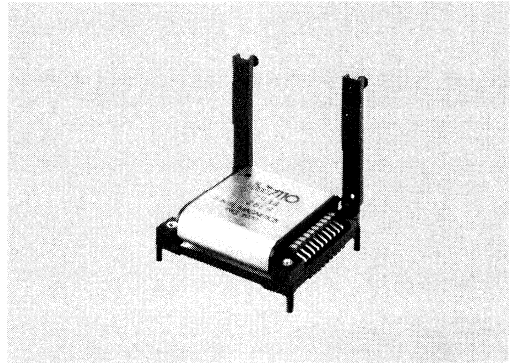
Bubbles, following replication, are propagated along the output track to a detector that operates on the magneto-resistance principle. The cylindrical bubble domains are stretched into long strip domains by a chevron expander and are then propagated to the active portion of the detector. The detector consists of a stack of interconnected chevrons through which a current is passed. As the strip domain propagates through the stack, its magnetic flux causes a fractional change in stack resistance which produces an output signal on the order of a few millivolts. The strip domain following detection is propagated to a bubble bucket guard rail. A "dummy" detector stack sits in the immediate vicinity. It is connected in series with the active detector and serves to cancel common mode pickup which originates predominately from the in-plane drive field.

6) Boot Loop, Boot Swap, and Boot Replicate

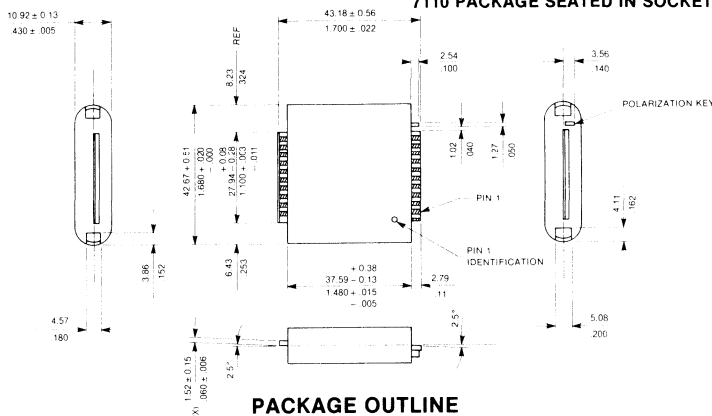
One of the two quads in each half chip contains a functionally active Boot Storage Loop. This loop is used to store:

- A loop mask code that defines which loops within the main storage area should be accessed. Faulty loops are "masked out" by the support electronics.
- A synchronization code that assigns data addresses (pages) to the data in the storage loops. Since bubbles move from one storage location to the next every field rotation, the actual physical location of a page of data is determined by the number of field rotations that have elapsed with respect to a reference.

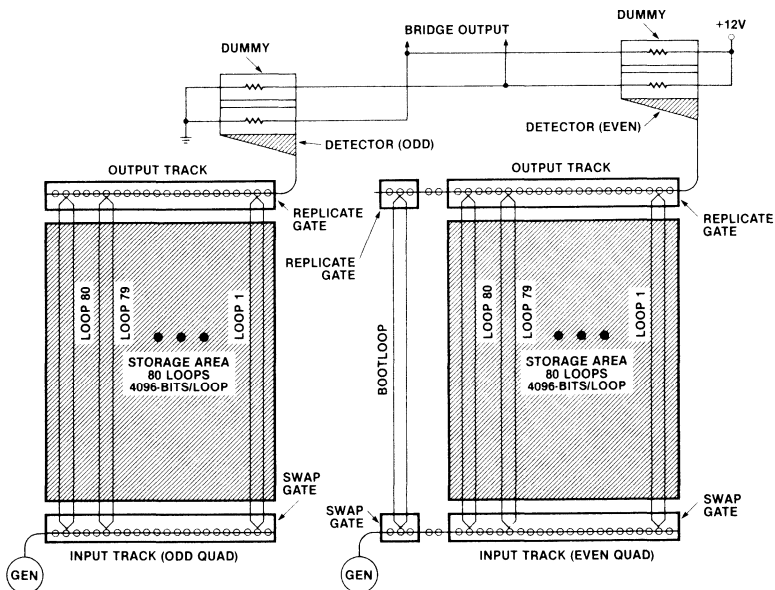
The boot loop is read from and written into via the same input and output tracks as the main storage loops. However, it has independently accessed swap and replicate gates. The boot swap, under normal circumstances, is intended only to be used during basic initialization at the factory at which time loop mask and synchronization codes are written. The boot replicate is intended to be accessed every time power is applied to the bubble module and its peripheral control electronics. At such a time, the control electronics would read and store the mask information, plus utilize the synchronization information to establish the location of the data circulating within the loops.



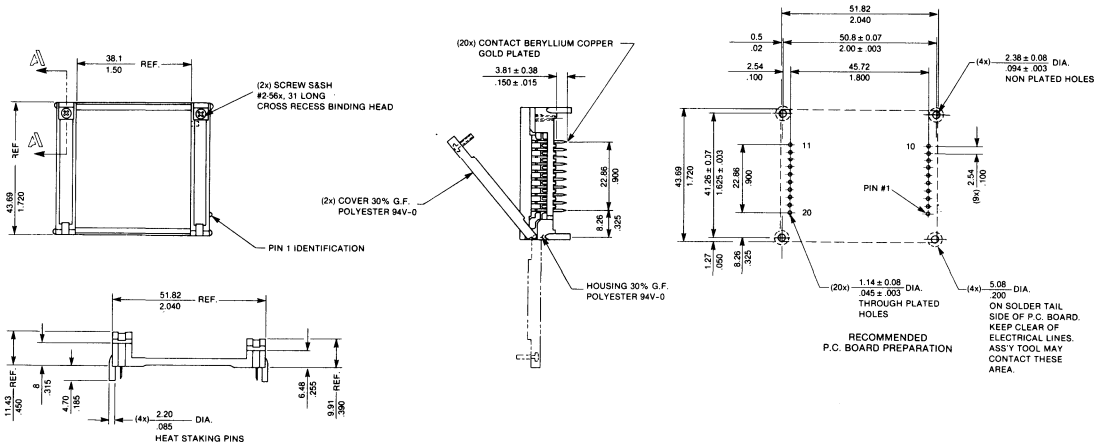
7110 PACKAGE SEATED IN SOCKET WITH ARMS UP



PACKAGE OUTLINE



MAJOR TRACK-MINOR LOOP ARCHITECTURE OF 7110 (ONE HALF SHOWN)



SOCKET OUTLINE

PIN DESCRIPTION

BOOT.REP (Pin 4)

Two-level current pulse input for reading the boot loop.

BOOT.SWAP (Pin 5)

Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM.

DET.COM (Pin 15)

Ground return for the detector bridge.

DET.OUT (Pins 16 through 19)

Differential pair (A+, A- and B+, B-) outputs which have signals of several millivolts peak amplitude.

DET.SUPPLY (Pin 20)

+12 volt supply pin.

GEN.A and GEN.B (Pins 7, 8)

Two-level current pulses for writing data onto the input track.

PULSE.COM (Pin 1)

+12 volt supply pin.

REP.A and REP.B (Pins 3 and 2)

Two-level current pulses for replicating data from storage loops to output track.

SWAP.A and SWAP.B (Pins 13, 14)

Single-level current pulse for swapping data from input track to storage loops.

X-.COIL.IN, X+.COIL.IN (Pins 9, 10)

Terminals for the X or inner coil.

Y-.COIL.IN, Y+.COIL.IN (Pins 11, 12)

Terminals for the Y or outer coil.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0-70°C
Relative Humidity	95%
Non-Volatile Storage Temperature	-40 to +100°C
Shelf Storage Temperature (Data Integrity Not Guaranteed)	-65°C to +150°C
Voltage Applied to DET.SUPPLY or PULSE.COM	14 Volts
Continuous Current between PULSE.COM and Inputs	13.0 Volts
Continuous Current between DET.COM and Detector Outputs	10 mA
Coil Current	0.5A D.C.
External Magnetic Field for Non-Volatile Storage	20 Oersteds
Non-Operating Handling Shock (without socket)	200G
Operating Vibration (2 Hz to 2 kHz with socket)	20G

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Nom. ^[1]	Max.		
R ₁	Resistance: PULSE.COM to REP.A or REP.B		20		ohms	
R ₂	Resistance: PULSE.COM to BOOT.REP		8		ohms	
R ₃	Resistance: PULSE.COM to BOOT.SWAP		17		ohms	
R ₄	Resistance: PULSE.COM to GEN.A or GEN.B		32		ohms	
R ₅	Resistance: PULSE.COM to SWAP.A or SWAP.B		120		ohms	
R ₆	Resistance: DET.COM to DET.OUT.A+ or DET.OUT.B+		640		ohms	
R ₇	Resistance: DET.COM to DET.OUT.A- or DET.OUT.B-		670		ohms	
R ₈	Resistance: DET.COM to DET.SUPPLY		510		ohms	
R _X	X Coil Resistance		5.2		ohms	
R _Y	Y Coil Resistance		2.7		ohms	
L _X	X Coil Inductance		98.5		μH	
L _Y	Y Coil Inductance		79		μH	

DRIVE REQUIREMENTS
 $T_A =$ Range specified in Table 1.

Symbol	Parameter	Min.	Nom. ^[1]	Max.	Units
f _R	Field Rotation Frequency	49.95	50.000	50.05	KHz
φ _L	Phase Lag from Y.COIL to X.COIL	85	90	95	Degrees
I _{PX}	X.COIL Peak Current		600		mA
I _{PY}	Y.COIL Peak Current		750		mA
T _{DX}	X.COIL Positive Turn On Phase		270		Degrees
T _{1X}	X.COIL Positive Turn On Width		108		Degrees
T _{2X}	X.COIL Positive Decay Width		72		Degrees
T _{3X}	X.COIL Negative Turn On Width		108		Degrees
T _{4X}	X.COIL Negative Decay Width		72		Degrees
T _{DY}	Y.COIL Positive Turn On Phase		0		Degrees
T _{1Y}	Y.COIL Positive Turn On Width		108		Degrees
T _{2Y}	Y.COIL Positive Decay Width		72		Degrees
T _{3Y}	Y.COIL Negative Turn On Width		108		Degrees
T _{4Y}	Y.COIL Negative Decay Width		72		Degrees
P _T	Total Coil Power		1.3		Watt

Note: 1. Nominal values are at $T_A = 25^\circ\text{C}$.

CONTROL PULSE REQUIREMENTS

Nominal values at $T_A = 25^\circ\text{C}$. See Notes 2 and 3.

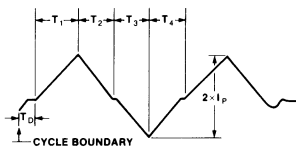
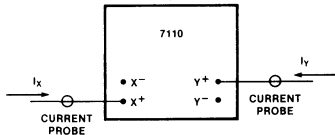
Pulse	Amplitude (mA)	Phase of Leading Edge (Degrees)	Width (Degrees)
GEN.A, GEN.B Cut	64	270 (Odd), 90 (Even)	4.5
GEN.A, GEN.B Transfer	36	270 (Odd), 90 (Even)	90
REP.A, REP.B Cut	180	270	4.5
REP.A, REP.B Transfer	140	270	90
SWAP	120	180	517
BOOT.REP Cut	90	270	4.5
BOOT.REP Transfer	70	270	90
BOOT.SWAP	70	180	See Note 4.

Note: 2. Pulse timing is given in terms of the phase relations as shown below. For example, a 7110 operating at $f_R = 50.000\text{ kHz}$ would have a REP.A transfer width of 90° which is $5\ \mu\text{s}$.

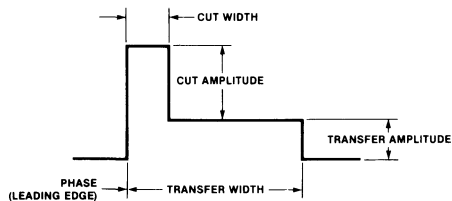
Table 1. 7110 Family

Part Number	T_A Range
7110	$0\text{--}50^\circ\text{C}$
7110-1	$0\text{--}70^\circ\text{C}$
7110-2	$10\text{--}50^\circ\text{C}$

X-Y COIL WAVEFORMS



3. Two level pulses are described as shown below.



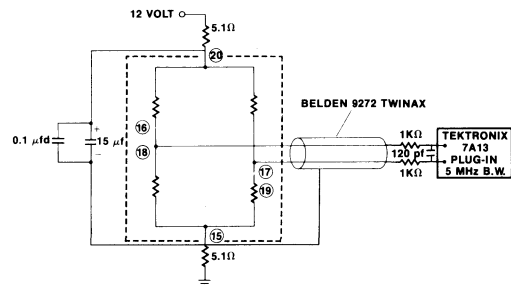
4. BOOT.SWAP is not normally accessed during operation. It is utilized at the factory to write the index address and redundant loop information into the bootstrap loops before shipment.

OUTPUT CHARACTERISTICS

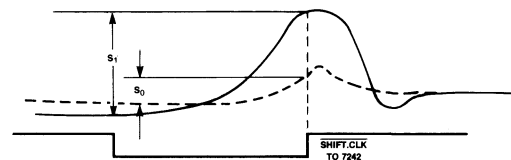
$T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Min.	Nom.	Max.	Units	Test Conditions
S_1		6		mV	See Figures below.
S_0		1		mV	

TEST SET-UP FOR OUTPUT VOLTAGE MEASUREMENT



DETECTOR OUTPUT WAVEFORMS



7220BRD BUBBLE MEMORY CONTROLLER

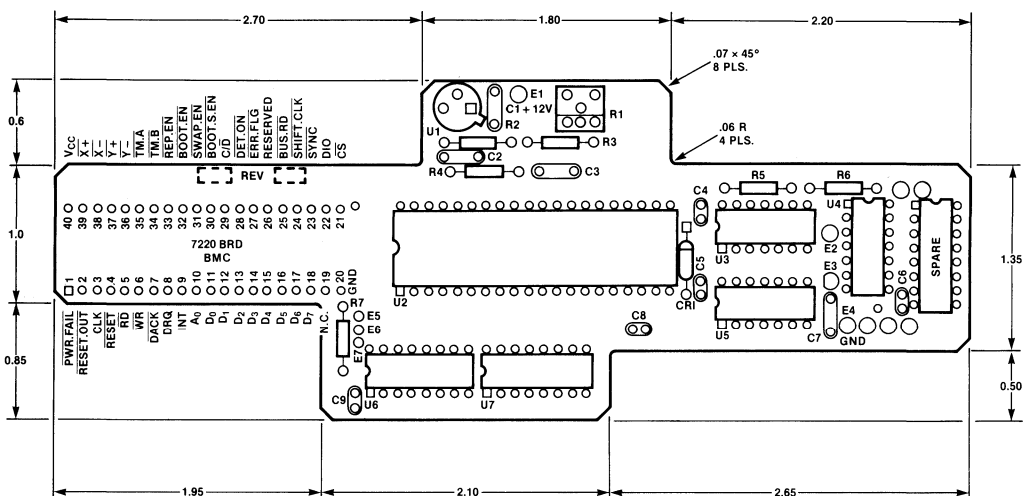
- 8080/8085/8088/8086 Microprocessor Interface
 - Interfaces Up to Eight BPK70 Bubble Storage Subsystems
 - Self-Contained Timing
- DMA Handshake Capability
 - Single or Multiple Page Block Transfers
 - Plug Directly Into a Standard 40-Pin Dual In-Line Socket

The Intel[®]7220BRD is a complete Bubble Memory Controller (BMC) designed to provide the interface between Intel Bubble Memories and standard microprocessors such as the 8080, 8085, 8088 and 8086.

The 7220BRD has self-contained timing generation and DMA handshake capability. Single and/or multiple page block transfers are also possible.

The 7220BRD is capable of interfacing with up to eight BPK70 one megabit bubble storage subsystems.

The 7220BRD uses Intel's high performance HMOS technology. The 7220BRD is a fully assembled printed circuit board, designed to plug into a standard 40-pin dual in-line socket. All inputs and outputs are directly TTL compatible. The 7220BRD requires two voltages: +5 Vdc and +12 Vdc.



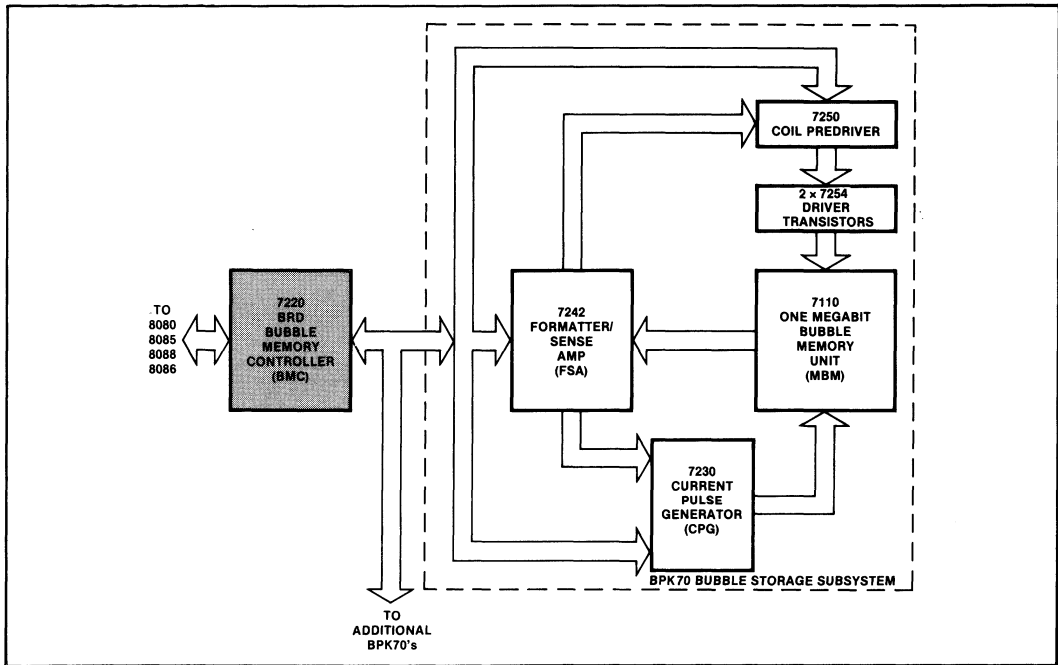


Figure 1. Block Diagram of Single Bubble Storage System — 128K Bytes and Pin Configuration

HARDWARE DESCRIPTION

The 7220BRD Bubble Memory Controller Board consists of a single printed circuit board, a 7220 Bubble Memory

Controller, and support circuits. The 7220BRD printed circuit board is designed to plug into a standard 40-pin dual in-line socket. The following table lists the individual pins and describes their function.

Table 1. Pin Description

Signal Name	Pin No.	I/O	Source/Destination	Description
V _{CC}	40			+5 Vdc Supply to support circuits
+12	E1			+12 Vdc used by 7220 BMC on-board regulator
GND	20 and E4		(ground)	+12/+5V return
PWR.FAIL	1	I	7230 CPG	A low forces a controlled stop sequence and holds THE BMC in an IDLE state (similar to RESET).
RESET.OUT	2	O	7250 CPD/7242 FSA 7230 Reference Current Switch	An active low signal to disable external logic initiated by PWR.FAIL or RESET signals, but not active until a stopping point in a field rotation is reached (if the BMC is causing the bubble memory drive field to be rotated).
CLK	3	I	Host Bus	4 MHz, TTL-level clock.
RESET	4	I	Host Bus	A low on this pin forces the interruption of any BMC sequencer activity, performs a controlled shut-down, and initiates a reset sequence. After the reset sequence is concluded, a low on this pin causes a low on the RESET.OUT pin. After a reset sequence has been run, the next BMC sequencer command must be the Initialize command.

Table 1. Pin Description (Continued)

Signal Name	Pin No.	I/O	Source/Destination	Description
RD	5	I	Host Bus	A low on this pin enables the BMC output data to be transferred to the host data bus (D ₀ -D ₇).
WR	6	I	Host Bus	A low on this pin enables the contents of the host data bus (D ₀ -D ₇) to be transferred to the BMC.
DACK	7	I	Host Bus	A low signal is a DMA acknowledge. This notifies the BMC that the next memory cycle is available to transfer data. This line should be active only when DMA transfer is desired and the DMA ENABLE bit has been set. CS should not be active during DMA transfers except to read status. DACK requires an external 1K ohm pullup resistor to +5V if DMA is not used.
DRQ	8	O	Host Bus	A high on this pin indicates that a data transfer between the BMC and the host memory is being requested.
INT	9	O	Host Bus	A high on this pin indicates that the BMC has a new status and requires servicing when enabled by the host CPU.
A ₀	10	I	Host Bus	A high on this pin selects the command/status registers. A low on this pin selects the data register.
D ₀ -D ₇	11-18	I/O	Host Bus	Host CPU data bus. An eight-bit bidirectional port which can be read or written by using the RD and WR strobes. D ₀ shall be the LSB.
D ₈	19			No connect
CS	21	I	Host Bus	Chip Select Input. A high on this pin shall disable the device to all but DMA transfers (i.e., it ignores bus activity and goes into a high impedance state).
DIO	23	O	7242 FSA	A bidirectional active high data line that shall be used for serial communications with 7242 FSA devices.
SYNC	23	O	7242 FSA	An active low output utilized to create time division multiplexing slots in a 7242 FSA chain. It shall also indicate the beginning of a data or command transfer between BMC and 7242 FSA.
SHIFT.CLK	24	O	7242 FSA	A controller generated clock that initiates data transfer between selected FSAs and their corresponding bubble memory devices. The timing of SHIFT.CLK shall vary depending upon whether data is being read or written to the bubble memory.
BUS.RD	25	O	*	An active low signal that indicates that the DIO line is in the output mode. It shall be used to allow off-board expansion of 7242 FSA devices.
WAIT	26	I/O	*	Reserved. (Requires an external pullup resistor which is >5K ohm to V _{CC} .)
ERR.FLG	27	I	7242 FSA	An active low input generated externally by 7242 FSA indicating that an error condition exists. Note: The 7242 ERR.FLG driver is open drain. (Requires an external pullup resistor which is >5K ohm to V _{CC} .)

*Not used in minimum (1M byte) system.

Table 1. Pin Description (Continued)

Signal Name	Pin No.	I/O	Source/Destination	Description
$\overline{\text{DET.ON}}$	28	O	*	An active low signal that indicates the system is in the read mode and may be detecting. It is useful for power saving in the MBM.
C/D	29	O	7242 FSA	A high on this line indicates that the BMC is beginning an FSA command sequence. A low on this line indicates that the BMC is beginning a data transmit or receive sequence.
$\overline{\text{BOOT.SW.EN}}$	30	O	7230 CPG	An active low signal which may be used for enabling the $\overline{\text{BOOT.SWAP}}$ of the 7230 CPG.
$\overline{\text{SWAP.EN}}$	31	O	7230 CPG	An active low signal used to create the swap function in external circuits.
$\overline{\text{BOOT.EN}}$	32	O	7230 CPG	An active low signal enabling the bootstrap loop replicate function in external circuitry.
$\overline{\text{REP.EN}}$	33	O	7230 CPG	An active low signal used to enable the replicate function in external circuitry.
$\overline{\text{TM.B}}$	34	O	7230 CPG	An active low timing signal generated by the decoder logic for determining TRANSFER pulse width.
$\overline{\text{TM.A}}$	35	O	7230 CPG	An active low timing signal generated by the decoder logic for determining CUT pulse width.
$\overline{\text{Y-}}, \overline{\text{Y+}},$ $\overline{\text{X-}}, \overline{\text{X+}}$	36-39	O	7250 CPD	Four active low timing signals generated by the decoding logic and used to create coil drive currents in the bubble memory device.
$\overline{\text{RD.SYNC}}$	E2	O		Reserved.
$\overline{\text{DIS.TXCVR}}$	E3	O		Reserved.

*Not used in minimum (1M byte) system.

FUNCTIONAL DESCRIPTION

The 7220BRD Bubble Memory Controller provides the user interface to the bubble memory system. The 7220BRD generates all memory system timing and control, maintains memory address information, interprets and executes user request for data transfers, and provides a Microprocessor-Bus compatible interface for the magnetic bubble memory system.

Figure 2 is a block diagram of the 7220BRD Bubble Memory Controller (BMC). The following paragraphs describe the functions of the individual elements of the BMC.

System Bus Interface—The System Bus Interface (SBI) logic contains the timing and control logic required to interface the BMC to a non-multiplexed bus. The interface has input data, output data, and status data latches. With a 4-MHz clock, it is capable of sustaining a 1.0 Mbyte per second transfer rate, while data space is available in the BMC FIFO. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes to the system bus interface must be synchronized with the 7220 clock (4 MHz). This is done in the SYNC RESOLVER section of the 7220BRD.

FIFO—The FIFO consists of a 40 × 8 bit FIFO RAM for

data storage. The FIFO block also contains input and output data latches, providing double data buffering, to improve the R/W cycle times seen at the system bus interface. The FIFO may be used as a general purpose FIFO when a command is not being executed by the 7220BRD Sequencer. In this mode, the FIFO READY status bit becomes a FIFO not-empty indicator indicating that the RAM and input/output latches have at least one byte of data.

DMA and Interrupt Logic—The DRQ pin has two functions:

- (1) If the DMA enable bit in the enable register is set, the DRQ pin, in conjunction with the $\overline{\text{DACK}}$ pin, provides a standard DMA transfer capability; i.e., it has the ability to handshake with an 8257 or 9517/8237 DMA controller chip.
- (2) If the DMA enable bit is reset, the DRQ pin acts as a “ready for data transfer interrupt” pin. It becomes active when 22 bytes may be read from or written into the BMC; it is reset when this condition no longer exists.

Register File—The register file contains 7 eight-bit registers that are accessible by the host CPU. Refer to the Register Section for details.

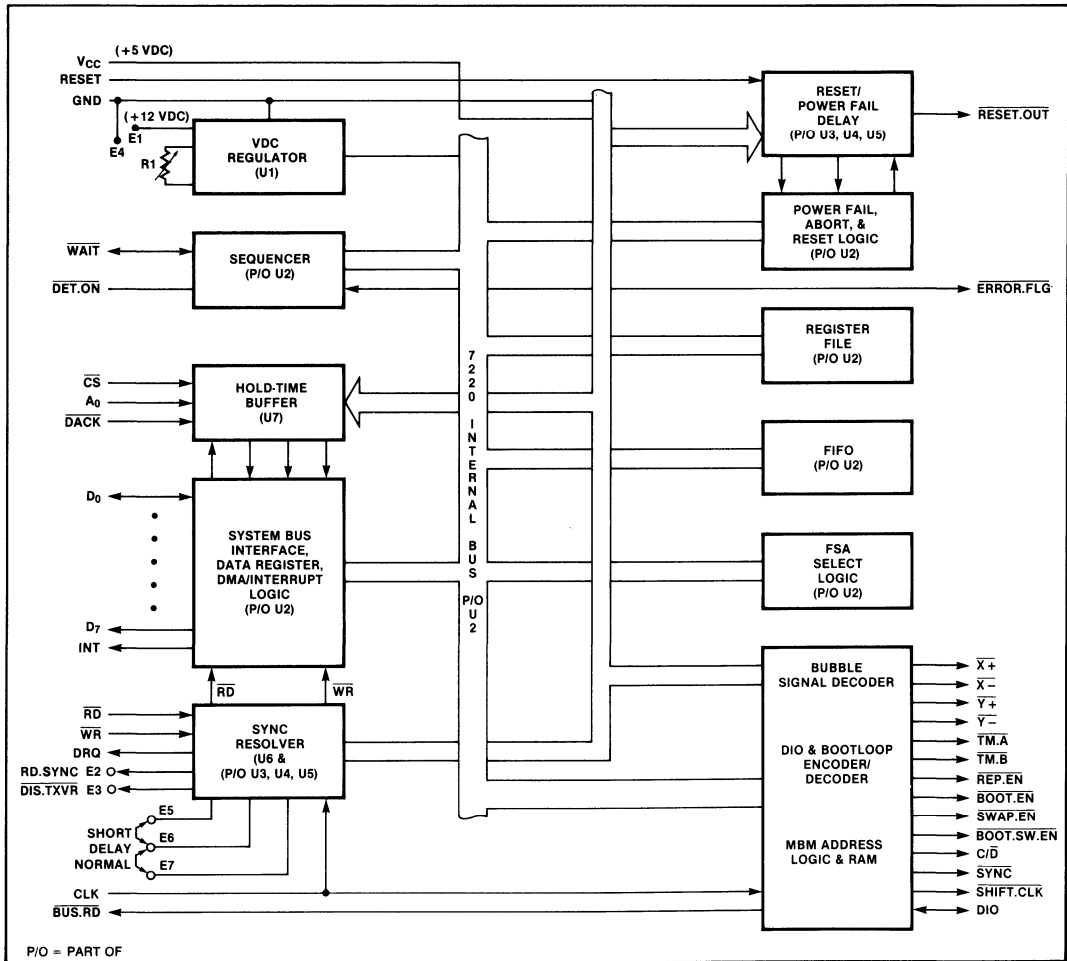


Figure 2. 7220BRD Bubble Memory Controller, Block Diagram

MBM Address Logic and RAM—The MBM address logic consists of the block length counter, starting address counter, adder, and MBM Address RAM. The MBM Address RAM is used to store the next available page address for each of up to 8 dual FSAs. The address maintained is the read address, the write address is generated when needed by adding a constant to the stored read address.

The block length counter enables multiple page transfers of up to 2047 pages in length.

The starting address counter is used as a register to hold the desired start address. Once the start address is reached, the counter is incremented on each subsequent page transfer so that its value is equal to the present read/write address.

DIO Bootloop Decoder/Encoder—Performs parallel-to-serial and serial-to-parallel conversions between the FIFO data and the serial bit stream on the DIO line. This block also generates the BUS.RD signal, which indicates the direction of data transfer on the DIO line (this is useful in situations which require external buffering on the DIO line). This block also contains the circuitry which decodes the bootloop data during a Read Bootloop or Initialize operation, and encodes the bootloop data during a Write Bootloop operation.

Sequencer—Controls the execution of commands by decoding the contents of its own internal ROM in which the 7220BRD firmware is located. This block also sets and resets flags and status bits, and controls actions in other parts of the 7220BRD.

Power Fail and Reset—Provides a means of resetting the bubble systems in an orderly manner, when activated by Power up, Power fail or during Reset.

FSA Select Logic block contains the logic which controls the timing of the interaction between the BMC and the FSAs. The FSA selection is determined by the four high-order bits in the BLR and the four high-order bits in the AR, both set by the user.

Sync Resolver consists of delay and resynchronizing logic for the read and write timing signals. Jumper option E5-E6 selects normal \overline{WR} delay. Jumper option E6-E7 selects \overline{WR} delayed one additional clock period.

Hold-Time Buffer inhibits changing of \overline{CS} , A_0 , and \overline{DACK} state after a read strobe RD.

Bubble Signal Decoder block contains the logic for creating all the MBM timing signals. The BMC to bubble memory interface consists of active low timing signals. The starting and stopping point of each signal is determined by the decoder logic. Each signal may occur every field rotation or only once in a number of field rotations. The field rotation in which a timing pulse occurs is controlled by the sequencer logic.

Voltage REGULATOR supplies voltage to 7220 BMC integrated circuit (U2-40). Regulator output is adjusted by potentiometer R1. (Set at factory.)

Figure 3 and Table 2 illustrate the typical timing signals for the BMC. These signals are described in the following paragraphs.

$\overline{X+}$, $\overline{X-}$, $\overline{Y+}$, and $\overline{Y-}$ go to the 7250 CPDs, and are used to enable the coil drive currents in the MBMs.

Table 2. 7220BRD BMC Timing (Degrees)

Signal	Start	Width	End
$\overline{X+}$	270°	108°	378°
$\overline{Y+}$	0°	108°	108°
$\overline{X-}$	90°	108°	198°
$\overline{Y-}$	180°	108°	288°
$\overline{TM.A}$ (ODD)	270°	4.5°	274.5°
$\overline{TM.A}$ (EVEN)	90°	4.5°	94.5°
$\overline{TM.B}$ (ODD)	270°	90°	360°
$\overline{TM.B}$ (EVEN)	90°	90°	180°
$\overline{BOOT.EN}$	252°	108°	360°
$\overline{REP.EN}$	252°	108°	360°
$\overline{SWAP.EN}$	180°	517°	697°
$\overline{BOOT.SW.EN}$	180°	DC*	180°
$\overline{SHIFTCLK}$ (RD)	186.75°	99°	285.75°
$\overline{SHIFTCLK}$ (WRT)	72°	288°	360°

*Stays low for 4118 field rotation periods when writing the MBM Bootloop.

$\overline{TM.A}$ and $\overline{TM.B}$ go to the 7230 CPGs, and are used to determine, respectively, the pulse widths for the CUT and TRANSFER functions used in replicating and generating the bubbles.

$\overline{SWAP.EN}$, $\overline{REP.EN}$, $\overline{BOOT.SW.EN}$, and $\overline{BOOT.EN}$ all go to the 7230 CPG. They are used to enable, respectively, the data swap, data replicate, boot swap, and boot replicate functions within the MBMs.

$\overline{SHIFT.CLK}$ goes to the FSAs. It is used to control the timing of events at the interface between each FSA and its corresponding MBM. (Refer to 7242 FSA Specification for a description of the BMC/FSA interface.)

\overline{SYNC} and $\overline{C/D}$ control the serial communications between the BMC and the FSAs (on the DIO line).

USER-ACCESSIBLE REGISTERS

The user operates the bubble memory system by reading from or writing to specific registers within the bubble memory controller (BMC). The following paragraphs identify these registers and gives brief functional descriptions, including bit configurations and address assignments.

Register Addressing

Selection of the user-accessible registers depends on register address information sent from the user to the 7220BRD. This address information is sent via a single address line (designated A_0) and also via data lines D_0 through D_4 .

Both Command Register (CMDR) and Register Address Counter (RAC) are 4-bit registers which are loaded from D_0 - D_3 . The status register is selected and read by a single read request. The command register is selected and loaded by a single write request. The remaining registers are accessed by a two-stage process, in which the desired register is first selected by placing its address in the RAC, and then read or written with a subsequent read or write request. Table 3 gives a complete listing of the address assignments for the user-accessible registers. The registers are listed in two groups. The first group (STR, CMDR, RAC) consists of those registers that are selected and accessed in one operation. The second group (UR, BLR, ER, AR, FIFO) consists of those registers that are selected according to the contents of RAC.

The register file contains the registers with address 1010 through 1111. These registers are also called parametric registers because they contain flags and parameters that determine exactly how the BMC will respond to commands written to the CMDR. To facilitate such operations, the BMC automatically increments the RAC by one count after each transfer of data to or from a parametric register.

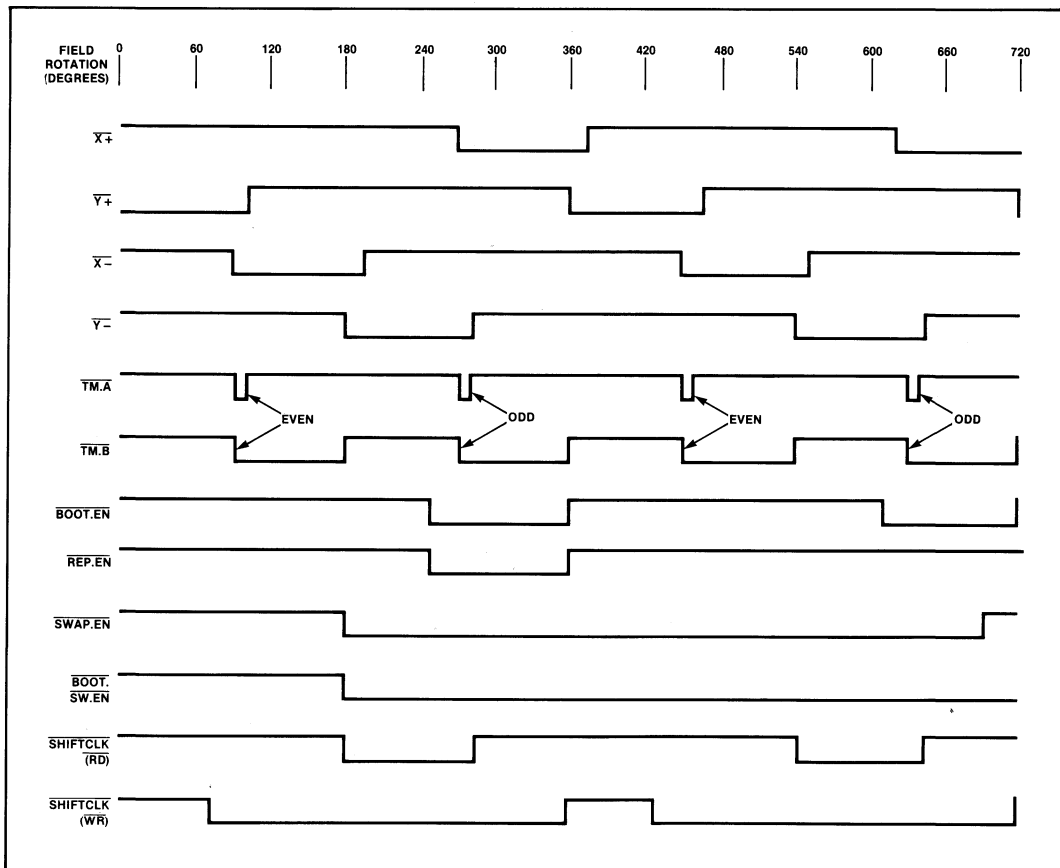


Figure 3. 7220BMC Timing Diagram

The RAC increments from the initially loaded value through address 1111 and then on to 0000 (the FIFO address). When it has reached 0000, it no longer increments. All subsequent data transfers (with A0=0) will be to or from the FIFO until such time as the RAC is loaded with a different register address.

Table 3. Address Assignments for the User-Accessible Registers

A0	D7	D6	D5	D4	D3	D2	D1	D0	Symbol	Name of Register	Read/Write
1	0	0	0	1	C	C	C	C	CMDR	Command Register	Write Only
1	0	0	0	0	B	B	B	B	RAC	Register Address Counter	Write Only
1	S	S	S	S	S	S	S	S	STR	Status Register	Read Only

Table 3. (Continued)

RAC					Symbol	Name of Register	Read/Write
A0	B3	B2	B1	B0			
0	1	0	1	0	UR	Utility Register	Read or Write
0	1	0	1	1	BLR LSB	Block Length Register LSB	Write Only
0	1	1	0	0	BLR MSB	Block Length Register MSB	Write Only
0	1	1	0	1	ER	Enable Register	Write Only
0	1	1	1	0	AR LSB	Address Register LSB	Read or Write
0	1	1	1	1	AR MSB	Address Register MSB	Read or Write
0	0	0	0	0	FIFO	FIFO Data Buffer	Read or Write

SSSSSSSS = 8-bit status information returned to the user from the STR
 CCCC = 4-bit command code sent to the CMDR by the user.
 BBBB = 4-bit register address sent to the RAC by the user.
 B3B2B1B0 = 4-bit contents of RAC at the time the user makes a read or write request with A0=0.
 LSB = Least Significant Byte
 MSB = Most Significant Byte

REGISTER DESCRIPTIONS

Command Register (CMDR) 4 Bits, Write Only

The user issues a command to the BMC by writing a 4-bit command code to the CMDR. Table 4 lists the 4-bit command codes used to issue the sixteen commands recognized by the BMC. Table 5 is a listing of the commands and their function. Commands relating to the bootloop are used only for diagnostic purposes and not commonly used in normal operation.

Table 4. Command Code Definitions

D3	D2	D1	D0	Command Name
0	0	0	0	Write Bootloop Register Masked
0	0	0	1	Initialize
0	0	1	0	Read Bubble Data
0	0	1	1	Write Bubble Data
0	1	0	0	Read Seek
0	1	0	1	Read Bootloop Register
0	1	1	0	Write Bootloop Register
0	1	1	1	Write Bootloop
1	0	0	0	Read FSA Status
1	0	0	1	Abort
1	0	1	0	Write Seek
1	0	1	1	Read Bootloop
1	1	0	0	Read Corrected Data
1	1	0	1	Reset FIFO
1	1	1	0	MBM Purge
1	1	1	1	Software Reset

Table 5. 7220BRD Commands

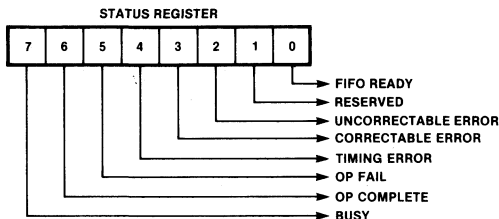
Initialize	The BMC executes the Initialize command by first interrogating the bubble system to determine how many FSAs are present, then reading and decoding the bootloop from each MBM and storing the results in the corresponding FSA's bootloop register. All the parametric registers must be properly set up before issuing the Initialize command.
Read Bubble Data	The Read Bubble Data command causes data to be read from the MBMs into the BMC FIFO. The selection of the MBMs to be accessed and the starting address for the read operation is specified in the address register (AR). The block length register (BLR) specifies the number of system pages to be read. All the parametric registers must be properly set up before issuing the Read Bubble Data command.
Write Bubble Data	The Write Bubble Data command causes data to be read from the BMC FIFO and written into the MBMs. The selection of the MBMs to be accessed and the starting address for the write operation is specified in the address register (AR). The block length register (BLR) specifies the number of system pages to be written. All the parametric registers must be properly set up before issuing the Write Bubble Data command.
Read Seek	The Read Seek command rotates the selected MBMs to a designated page address location. No data transfer occurs. The positioning is such that the next data location available to be read is the specified (in AR) page address plus one. The Read Seek command may be used to reduce latency (access time) in cases where information is available for the user to predict the location of an impending read reference to the MBMs.
Write Seek	The Write Seek command rotates the selected MBMs to a designated page address location. No data transfer occurs. The positioning is such that the next data location available to be written is the specified (in AR) page address plus one. The Write Seek command may be used to reduce latency (access time) in cases where information is available for the user to predict the location of an impending write reference to the MBMs.
Abort	The Abort command should not be used, it may cause loss of Bubble data.
MBM Purge	The MBM Purge command clears all BMC registers, counters, and the MBM address RAM. Furthermore, it determines how many FSA channels are present in the system and stores this value in the 7220BRD. The "INITIALIZE" command uses this command as a subroutine.
Read Corrected Data	The Read Corrected Data command causes the BMC to read into the BMC FIFO a 256-bit block of data from the FIFO of each selected FSA channel, after an error has been detected. The data cycles through the error correction network of the FSA. After the data has been read, the FSA reports to the BMC whether or not the error was correctable. The Read Corrected Data command is used only when the system is in error correction mode (ENABLE ICD or ENABLE RCD set in the ER).

Table 5. 7220BRD Commands (Continued)

Software Reset	The Software Reset command clears the BMC FIFO and all registers, except those containing initialization parameters. It also causes the BMC to send the Software Reset command to selected FSAs in the system. No reinitialization is needed after this command.
Read FSA Status	The Read FSA Status command causes the BMC to read the 8-bit status register of all FSAs, and to store this information in the BMC FIFO. The Read FSA Status command is independent of all parametric registers.
Read Bootloop Register	The Read Bootloop Register command causes the BMC to read the bootloop register of the selected FSA channels and to store this information in the BMC FIFO. Twenty bytes are transferred for each FSA channel selected.
Write Bootloop Register	The Write Bootloop Register command causes the BMC to write the contents of the BMC FIFO into the bootloop register(s) of the selected FSA channels. Twenty bytes are needed for each FSA channel selected.
Write Bootloop Register Masked	Proper operation of the FSAs during data transfer to or from the MBMs requires that the bootloop register contain (if error correction is used) exactly 270 logic 1s for each FSA bootloop register. The user may select any subset of 270 "good" loops from the total number of available loops (if error correction is not used, 270 replaced by 272). As an alternative, the Write Bootloop Register Masked command may be used. This command counts the number of logic 1s and masks out the remaining 1s after the proper count has been reached. The "INITIALIZE" command uses this command as a subroutine.
Read Bootloop	The Read Bootloop command causes the BMC to read the bootloop from the selected MBM, and to store the decoded bootloop information in the BMC FIFO. The "INITIALIZE" command uses this command as a subroutine.
Write Bootloop	The Write Bootloop command causes the existing contents of the selected MBM's bootloop to be replaced by new bootloop data based on 40 bytes of information stored in the FIFO (the user must actually write 41 bytes, where the 41st byte is all 0s). Encoding of the bootloop data is done by the BMC hardware.

Status Register (STR) 8 Bits, Read Only

The user reads the BMC status register in response to an interrupt signal, or as part of the polling process in a polled data transfer mode. The status register provides information about error conditions, completion or termination of commands, and about the BMC's readiness to transfer data or accept new commands. The individual bit descriptions are as follows:



BUSY (when = 1) indicates that the BMC is in the process of executing a command. When equal to 0, **BUSY** indicates that the BMC is ready to receive a new command. In the case of a read command, **BUSY** may also indicate that the data has not been completely removed from the FIFO, and that DRQ

is still active. **BUSY** will then drop as soon as DRQ does (after the user has finished reading the data remaining in the FIFO).

OP COMPLETE (when = 1) indicates the successful completion of a command.

OP FAIL (when = 1) indicates that an FSA has reported a timing error to the BMC, or that the host system has failed to keep up with the BMC, thereby causing the BMC FIFO to overflow or to become empty. **TIMING ERROR** is also set if no bootloop sync word is found during initialization, or if a Write Bootloop command is issued when the **WRITE BOOTLOOP ENABLE** bit is equal to zero in the enable register, and on "UNCORRECTABLE" error conditions. A software **RESET** command should be sent if any timing error condition arises.

CORRECTABLE ERROR (when = 1) indicates that a FSA has reported to the BMC that a correctable error has been detected in the last data block transferred.

UNCORRECTABLE ERROR (when = 1) indicates that an FSA has reported to the BMC that an uncorrectable error has been detected in the last data block transferred.

FIFO READY has two functions. The FIFO READY functions are as follows:

If RAC ≠ FIFO, FIFO READY = 1.

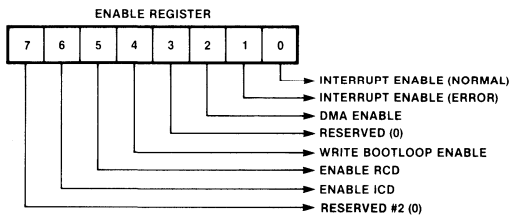
Status Bits (STR)		Read Mode	Write Mode
FIFO Ready	Busy		
1	1	data in FIFO	space in FIFO
0	1	no data	no space
1	0	— data in FIFO —	
0	0	— FIFO empty —	

Although the status word can be read at any time, the status information is not conclusive until the BUSY bit is low.

STR Bits 1 through 6 are reset when a new command is issued. They may also be reset by making a write request (WR=0) to the BMC with A₀=1, D₄=0, and D₅=1 (that is, writing the RAC with D₅=1). This operation also resets the "INT" pin to "0". NOTE: A byte of FIFO data can be lost if the RAC is written when data is still present in FIFO.

Enable Register (ER) 8 Bits, Write Only

The user sets various bits of the enable register to enable or disable various functions within the BMC or the FSAs. The individual bit descriptions are as follows:



In the above figure and in the text below, the following abbreviations are used:

- ICD = INTERNALLY CORRECT DATA
- RCD = READ CORRECTED DATA
- UCE = UNCORRECTABLE ERROR
- CE = CORRECTABLE ERROR
- TE = TIMING ERROR

Reserved #2 should always be loaded with 0.

ENABLE ICD enables the BMC to give the Internally Correct Data command to an FSA when an error has been detected by the FSA's error detection and correction circuitry. The FSA responds to such a command by internally cycling the data through its error correction network. When finished, the FSA returns status to the BMC as to whether or not the error is correctable. The value of ENABLE ICD affects the action of INTERRUPT ENABLE (ERROR).

ENABLE RCD enables the BMC to give the Read Corrected Data command to an FSA in which an error has been detected. This causes the FSA to correct the error (if possible) and also to transfer the corrected data to the BMC. The Read Corrected Data command is also used to read into the BMC data previously corrected by the FSA in response to an Internally Correct Data command. In either case, when the data transfer has been completed, the BMC can read FSA status to determine whether or not the error was correctable. In the case of an uncorrectable error, bad data may have been sent to the user. The value of ENABLE RCD affects the action of INTERRUPT ENABLE (ERROR).

WRITE BOOTLOOP ENABLE (when = 1) enables the bootloop to be written. If this bit is equal to zero, and a Write Bootloop command is received by the BMC, the command is aborted and the TIMING ERROR bit is set in the STR.

RESERVED should always be loaded to "0" in the 7220BRD.

DMA ENABLE (when = 1) enables the BMC to operate in DMA data transfer mode, using the DRQ and DACK signals in interaction with a DMA controller. When equal to zero, DMA ENABLE sets up the controller to support interrupt driven or polled data transfer.

INTERRUPT ENABLE (ERROR) selects error conditions under which the BMC stops command execution and interrupts the host processor (via the INT line). INTERRUPT ENABLE (ERROR) operates in conjunction with ENABLE ICD and ENABLE RCD.

Table 6. Summary of INTERRUPT ENABLE (ERROR) Bit

Enable ICD	Enable RCD	Interrupt Enable (ERROR)	Interrupt Action
0	0	0	No interrupts due to errors
0	0	1	Interrupt on TE only
0	1	0	Interrupt on UCE or TE
0	1	1	Interrupt on UCE, CE, or TE
1	0	0	Interrupt on UCE or TE
1	0	1	Interrupt on UCE, CE, or TE
1	1	0	Not used
1	1	1	Not used

TE — Timing Error
 CE — Correctable Error
 UCE — Uncorrectable Error

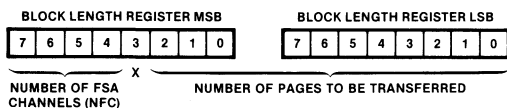
INTERRUPT ENABLE (NORMAL) (when = 1) enables the BMC to interrupt the host system (via the INT line), when a command execution has been successfully completed (OP COMPLETE = 1 in the STR).

Utility Register (UR) 8 Bits, Read or Write

The utility register is a general purpose register available to the user in connection with bubble memory system operations. It has no direct effect on the BMC operation, but is provided as a convenience to the user.

Block Length Register (BLR) 16 Bits, Write Only

The contents of the block length register determine the system page size and also the number of pages to be transferred in response to a single bubble data read or write command. The bit configuration is as follows:



The system page size is proportional to the number of magnetic bubble memory modules (MBMs) operating in parallel during the data read or write operation. Each MBM requires two FSA channels. Bits 4 through 7 of BLR MSB actually specify the number of FSA channels to be accessed.

The BLR LSB, together with the 3 least significant bits of the BLR MSB, specify the number of pages to be transferred. Up to 2047 pages can be transferred in response to a single bubble data read or write command, hence the requirement for 11 bits. All 11 bits equal to one specifies a 2047 page transfer.

Address Register (AR) 16 Bits, Read or Write

The contents of the address register determine which MBM group is to be accessed, and, within that group, what starting address location shall be used in a data read or write operation. The bit configuration is as follows:



Within each MBM there are 2048 possible starting address locations for a data read or write operation, hence the requirement for 11 bits in the starting address. The last page (page 2047) represented by all ones may not be read/written with the 7220BRD.

The selection of the MBMs to be read or written is specified by AR MSB Bits 3-6. The BMCs interpretation of these bits depends on the number of MBMs in a group, which is specified by BLR MSB Bits 4-7. Table 7 lists the MBMs in a group which is specified by BLR MSB Bits 4-7. Table 7 lists the MBM groups selected by the BLR MSB Bits 4-7 and AR MSB Bits 3-6. A one-megabyte system (eight MBMs) is represented, with the FSA channels numbered 0 through F:

Table 7. Selection of FSA Channels

AR MSB Bits (6,5,4,3)	BLR MSB Bits (7,6,5,4)				
	0000	0001	0010	0100	1000
0000	0	0,1	0,1,2,3	0 to 7	0 to F
0001	1	2,3	4,5,6,7	8 to F	
0010	2	4,5	8,9,A,B		
0011	3	6,7	C,D,E,F		
0100	4	8,9			
0101	5	A,B			
0110	6	C,D			
0111	7	E,F			
1000	8				
1001	9				
1010	A				
1011	B				
1100	C				
1101	D				
1110	E				
1111	F				

As explained above, the accessing of single FSA channels is done only as part of diagnostic processes. AR MSB Bit 7 is not used.

FIFO Data Buffer (FIFO) 40 x 8 Bits, Read or Write

The BMC FIFO is a 40-byte buffer through which data passes on its way from the FSAs to the user, or from the user to the FSAs. The FIFO allows the data transfer to proceed in an asynchronous and flexible manner, and relaxes timing constraints, both to the FSAs and also to the user's equipment. The user's system must, however, meet the data rate requirements. When the BMC is busy (executing a command) the FIFO functions as a data buffer. When the BMC is not busy, the FIFO is available to the user as a general purpose FIFO.

FUNCTIONAL OPERATION

The IC components used in the bubble memory system have been designed with transparency in mind—that is, a maximum number of operations are handled by the hardware and firmware of these components.

Each one-Megabit Bubble Memory (MBM) operates in its own domain, and is unaffected by the number of bubble memories in the system. The roles played by the MBM's immediate support circuitry can be described as if the system contained only one MBM module.

Data Flow Within the Magnetic Bubble Memory (MBM) System

During a read operation, data flows as follows: The data from the MBM is input to the Formatter/Sense Amplifier (FSA). Data from each channel (A channel or B channel) of the MBM goes to the corresponding channel of the FSA. In the FSA, the data is paired up with the corresponding bit in the FSA's bootloop register to determine whether it represents data from a 'good' loop. If it

does, the data bit is stored in the FSA FIFO. Error detection and correction (if enabled by the user) is applied to each block of 256 data bits.

From the FSA FIFO, data is sent to the bubble memory controller (BMC) in the form of a serial bit stream, via a one-line bidirectional data bus (DIO). The data is multiplexed onto the DIO line, with data bits coming alternately from the A and B channels of the FSA. The BMC outputs a $\overline{\text{SYNC}}$ pulse to the $\overline{\text{SELECT.IN}}$ input of the FSA. The FSA responds by placing a data bit from the A channel FIFO on the DIO line. One clock cycle later, a data bit from the B channel FIFO is placed on the DIO line. The BMC continues to output $\overline{\text{SYNC}}$ pulses, once every 80 clock cycles, each time receiving two data bits in return.

In the BMC, the data undergoes serial-to-parallel conversion, and is assembled into bytes, which are then placed in the BMC FIFO, which can hold 40 bytes of data. From this FIFO, the data bytes are written onto the user interface.

During a write operation, the data flow consists of the corresponding complementary operations in the reverse order.

Multiple-MBM Systems

The 7220 BMC can interface up to 8 one-megabit BPK-70 Bubble Storage subsystems. The data flow in a multiple-MBM system is in most respects similar to that which occurs in a one-MBM system. The difference is in the time-division multiplexing that occurs on the DIO bus line between the BMC and the FSAs.

For data transfer operations, the BMC may exchange data with as few as two FSA channels (one MBM) or as many as 16 FSA channels (eight MBMs).

SOFTWARE INTERFACE—The general procedure for communicating with the 7220BRD is:

- (1) Pass parameters to the 7220BRD by loading the registers.
- (2) Send the desired command.
- (3) Read/Write data to/from 7220BRD FIFO, if required, using one of the three data transfer modes.
- (4) Read the status register until BMC is not busy (or use "INT" pin).
- (5) Examine the status register to determine whether the operation was successful.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias - 10°C to + 80°C
 Storage Temperature - 65°C to + 150°C
 All Input or Output Voltages and
 V_{CC} Supply Voltage - 0.5V to 7V
 V_{DD} Supply Voltage - 0.5V to 14V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 50°C, V_{CC} = 5.0V +5%, -10%; V_{DD} = 12V ±5%)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V _{IL}	Input Low Voltage		0.8	V	
V _{IH}	Input High Voltage	2.0		V	
V _{OL(1)}	Output Low Voltage (All outputs except $\overline{\text{DET}}\text{ON}$, $\overline{\text{BUS}}\text{RD}$ $\overline{\text{SHIFT}}\text{CLK}$, and $\overline{\text{SELECT}}\text{OUT}$)		.45	V	I _{OL} = 3.2 mA
V _{OL(2)}	Output Low Voltage $\overline{\text{DET}}\text{ON}$, $\overline{\text{BUS}}\text{RD}$, $\overline{\text{SHIFT}}\text{CLK}$, $\overline{\text{SELECT}}\text{OUT}$.45	V	I _{OL} = 1.6 mA
V _{OH}	Output High Voltage	2.4		V	I _{OH} = 400 μA
I _{IL}	Input Leakage Current		10	μA	0 ≤ V _{IN} ≤ V _{CC}
I _{OFL}	Output Float Leakage		10	μA	0.45 ≤ V _{OUT} ≤ V _{CC}
I _{CC}	Power Supply Current from V _{CC}		50	mA	
I _{DD}	Power Supply Current from V _{DD}		200	mA	

A.C. CHARACTERISTICS (T_A = 0°C to +50°C, V_{CC} = 5.0V +5%, -10%;
 V_{DD} = 12V ±5%; C_L = 150 pF; unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
f _c	Clock Frequency	3.996	4.004	MHz	
t ₀	Clock Phase Width	0.45/f _c	0.55/f _c		
t _R -t _F	Input Signal Rise and Fall Time		30	ns	

FSA Interface Timings

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t _{CDV}	CLK to DIO Valid Delay		100	ns	
t _{CDF}	CLK to DIO Entering Float		220	ns	
t _{CDE}	CLK to DIO Enabled from Float		100	ns	
t _{CDH}	CLK to DIO Hold Time	0		ns	
t _{CSOL}	CLK to $\overline{\text{SELECT}}\text{OUT}$ Leading Edge Delay		100	ns	C _L = 50 pF
t _{CSOT}	CLK to $\overline{\text{SELECT}}\text{OUT}$ Trailing Edge Delay		100	ns	C _L = 50 pF
t _{DC}	DIO Setup Time to Clock	70		ns	
t _{DHC}	DIO Hold Time from Clock	0		ns	
t _{COL}	CLK to Output Leading Edge	150		ns	
t _{COT}	CLK to Output Trailing Edge	0		ns	
t _{EW}	$\overline{\text{ERR}}\text{.FLG}$ Pulse Width	200		ns	
t _{SCFT}	$\overline{\text{SHIFT}}\text{CLK}$ to $\overline{\text{Y}}$ - Trailing Edge	80	180	ns	

Read Cycle (Host Interface)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t _{AC}	Select Setup to \overline{RD}	0		ns	
t _{CA}	Select Hold from \overline{RD}	0		ns	
t _{RR}	\overline{RD} Pulse Width	500		ns	
t _{AD}	Data Delay from Address		450	ns	
t _{RD}	Data Delay from \overline{RD}		450	ns	
t _{DF}	Output Float Delay	270	350	ns	C _L = 20 pF for Min. 150 pF for Max.
t _{DC}	\overline{DACK} Setup to \overline{RD}	0		ns	
t _{CD}	\overline{DACK} Hold from \overline{RD}	0		ns	
t _{KD}	Data Delay from \overline{DACK}		450	ns	

Write Cycle (Host Interface)

t _{AC}	Select Setup to \overline{WR}	0		ns	
t _{CA}	Select Hold from \overline{WR}	0		ns	
t _{WW}	\overline{WR} Pulse Width	510 (760)		ns	Jumper E5-E6 (E6-E7)
t _{DW}	Data Setup to \overline{WR} t	50		ns	
t _{WD}	Data Hold from \overline{WR} t	10		ns	
t _{DC}	\overline{DACK} Setup to \overline{WR}	0		ns	
t _{CD}	\overline{DACK} Hold from \overline{WR}	10		ns	
t _{CQ}	Request Hold from \overline{RD} or \overline{WR} (non Burst mode)		150	ns	

7250-7230 Interface Timings

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t _{CBL}	CLK to Bubble Signal Leading Edge		200	ns	Under Pin Loads*
t _{CBT}	CLK to Bubble Signal Trailing Edge		200	ns	Under Pin Loads*

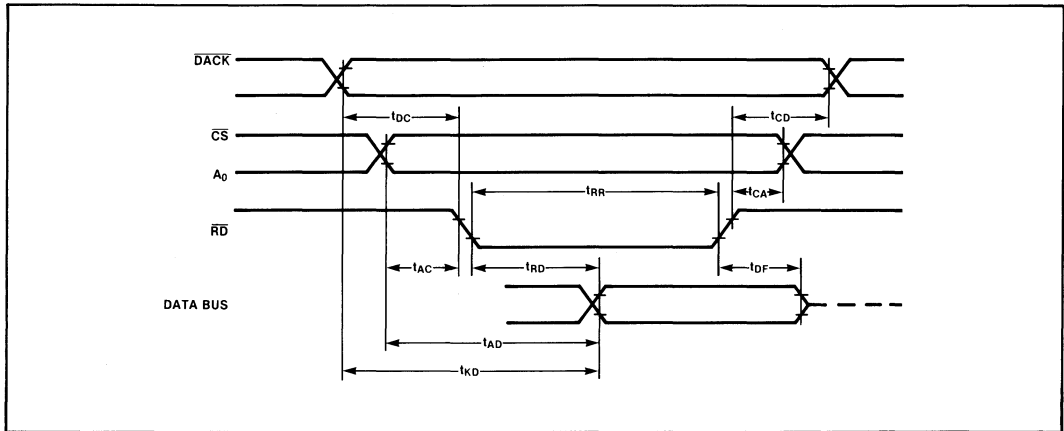
*Pin Loads Shown Below

PIN LOADINGS

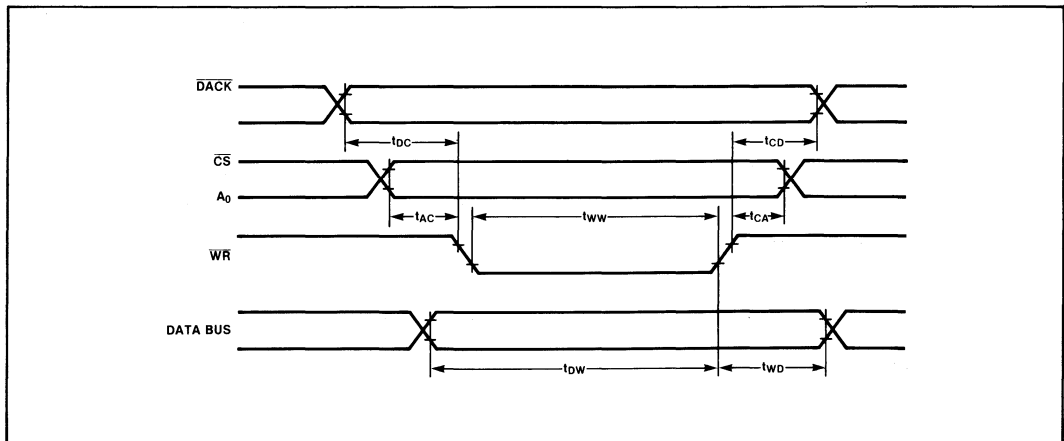
Pin Names	Value	Unit
$\overline{X+}$, $\overline{X-}$, $\overline{Y+}$, $\overline{Y-}$	150	pF
$\overline{TM.A}$, $\overline{TM.B}$, \overline{REPEN} , \overline{BOOTEN} , \overline{SWAPEN} , $\overline{BOOTSWEN}$, C/D, ERRFLG, WAIT, SYNC	50	pF
DET.ON & SHIFT.CLK	100	pF
BUS.RD	10	pF

WAVEFORMS

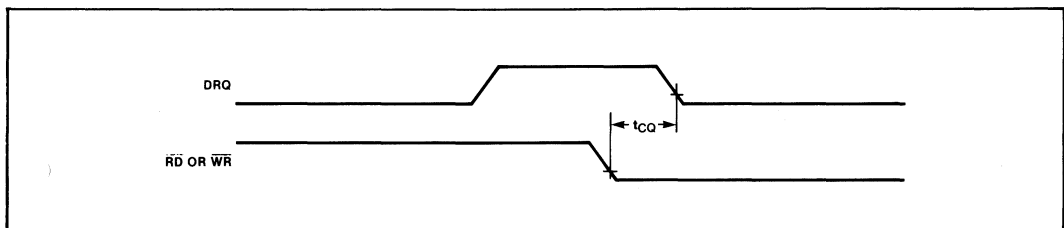
Read Waveforms (Host Interface)



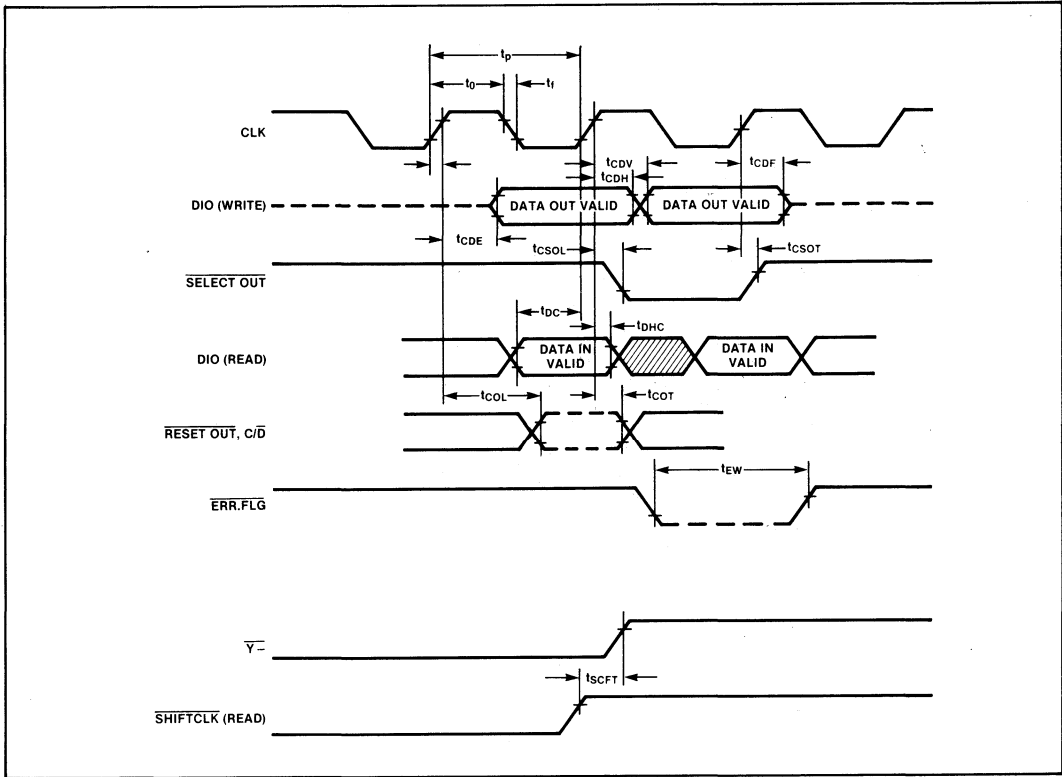
Write Waveforms (Host Interface)



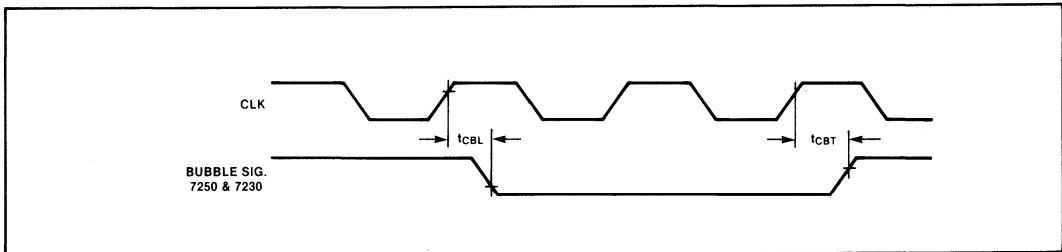
DMA Waveforms (Host Interface)



7242 Interface Timings



7250 & 7230 Interface Timings





7220COMP BUBBLE MEMORY CONTROLLER

- 8080/8085/8088/8086 Microprocessor Interface
- Interfaces Up to Eight Bubble Storage Subsystems
- Self-Contained Timing
- DMA Handshake Capability
- Single or Multiple Page Block Transfers
- Functionally Equivalent to 7220BRD
- Consisting of a Set of Components for Production Application

The Intel® 7220COMP is functionally equivalent to 7220BRD. It consists of a set of components for customers to incorporate onto their production boards. Please refer to the 7220BRD data sheet for 7220COMP specifications.

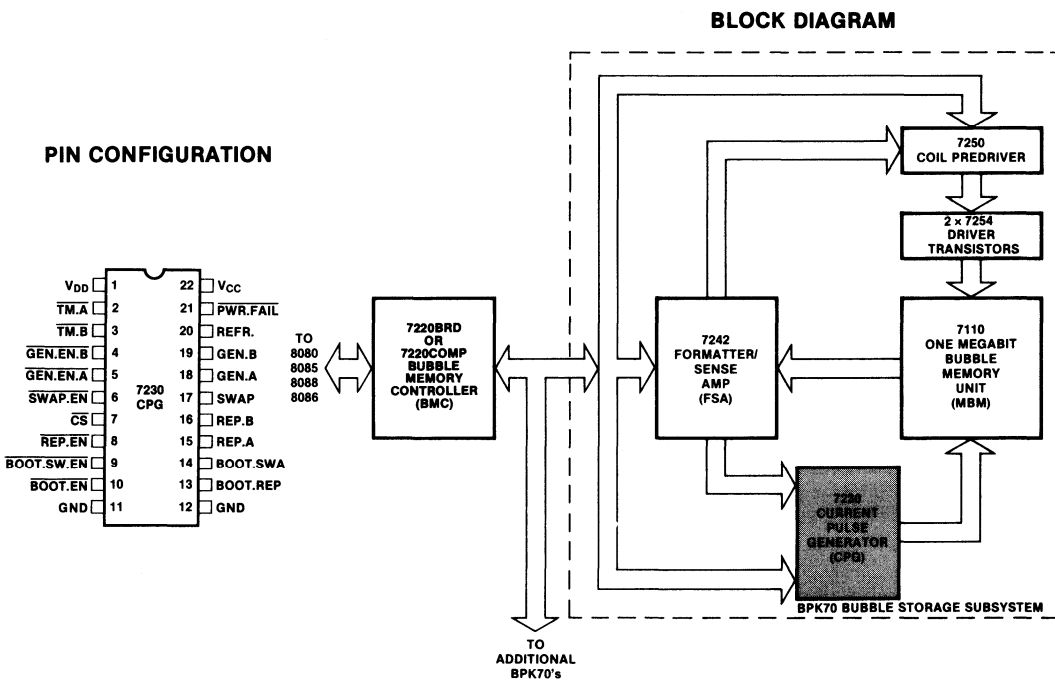


7230 CURRENT PULSE GENERATOR FOR BUBBLE MEMORIES

- TTL Compatible Inputs
- Provides all Pulses for IM's Bubble Memories
 - Replicate, Swap, Generate, Boot Replicate and Bootswap
- Current Sink Outputs Designed to Directly Drive Bubble Memory
- Direct Interface to Bubble Memory Controller
- Automatic Power Fail and Reset
- Operates from +5 and +12 Volts Only
- Schottky Bipolar Technology
- Standard 22-Pin Dual-In-Line Package

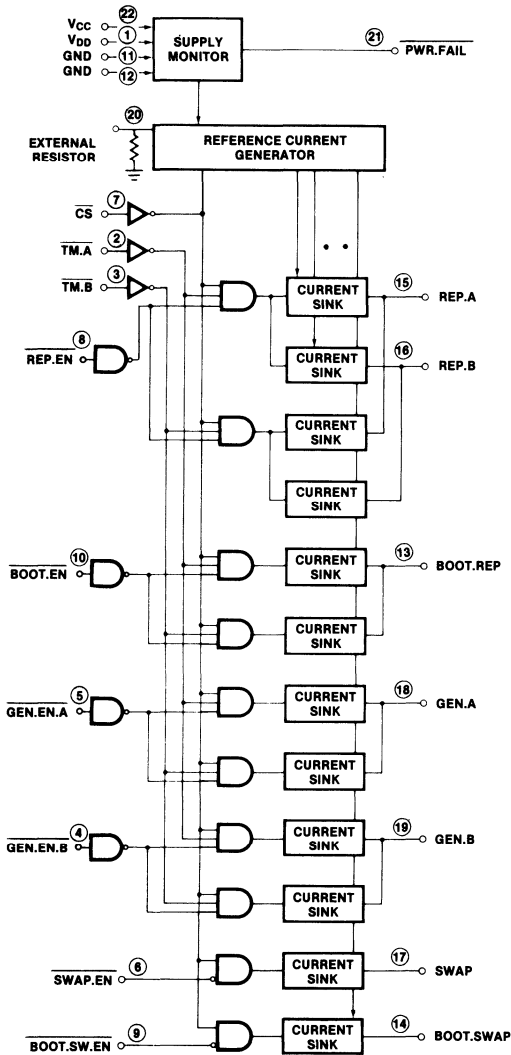
The Intel 7230 is a Current Pulse Generator (CPG) designed to drive Intel Magnetics Bubble Memories. The 7230 is a Schottky Bipolar, TTL input compatible device that converts digital timing signals to analog current pulses. The CPG provides all pulses for Intel Magnetics Bubble Memories (7110 Family). These include Replicate, Swap, Generate, Boot Replicate and Bootswap pulses. The high current sinking outputs directly drive the bubble memory. It also directly interfaces to the Intel Magnetics Bubble Memory Controller (7220) and Formatter/Sense amplifier (7242).

The 7230 operates from 5-volt and 12-volt power supplies and is in a standard 22-pin dual-in-line package.



Block Diagram of Single Bubble Memory System — 128K Bytes

LOGIC DIAGRAM



EXTERNAL RESISTOR REQUIREMENTS

Connect a 1% 3.48K ohm resistor based between pin 20 and ground or referenced current switch as outlined in BPK72 User's Manual

PIN DESCRIPTION

BOOT.EN (Pin 10)

An active low input enabling the BOOT.REP output current pulse.

BOOT.REP (Pin 13)

An output providing the current pulse for bootstrap loop replication in the bubble memory.

BOOT.SWAP (Pin 14)

An output providing a current pulse which may be used for writing data into the bootstrap loop.

BOOT.SW.EN (Pin 9)

An active low input enabling the BOOT.SWAP output current pulse.

CS (Pin 7)

An active low input for selecting the chip. The chip powers down during deselect.

GEN.A (Pin 18)

An output providing the current pulse for writing data into the "A" quads of the bubble memory.

GEN.B (Pin 19)

An output providing the current pulse for writing data into the "B" quads of the bubble memory.

GEN.EN.A (Pin 5)

An active low input enabling the GEN.A output current pulse.

GEN.EN.B (Pin 4)

An active low input enabling the GEN.B output current pulse.

PWR.FAIL (Pin 21)

An active low, open collector output indicating that either V_{CC} or V_{DD} is below its threshold value.

REFR. (Pin 20)

The pin for the reference current generator to which an external resistance must be connected.

REP.A (Pin 15)

An output providing the current pulse for replication of data in the "A" quads of the bubble memory.

REP.B (Pin 16)

An output providing the current pulse for replication of data in the "B" quads of the bubble memory.

REP.EN (Pin 8)

An active low input enabling the REP.A and REP.B outputs.

PIN DESCRIPTION (continued)
SWAP (Pin 17)

An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory.

SWAP.EN (Pin 6)

An active low input enabling the SWAP output.

TM.A (Pin 2)

An active low timing signal determining the cut pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

TM.B (Pin 3)

An active low timing signal determining the transfer pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias -20°C to +80°C
 Storage Temperature -65°C to +150°C
 V_{CC} and Input Voltages -0.5V to +7V
 V_{DD} and Output Voltages -0.5V to +13V
 Power Dissipation 1W
 Power Fail Output Sink Current 10 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} +5\%, -10\%$;
 $V_{DD} = 12\text{V} \pm 5\%$; unless otherwise specified)

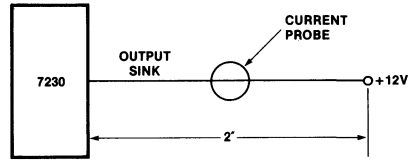
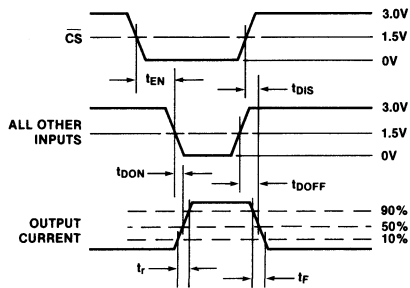
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{IL}	Input Low Current			-0.4	mA	$V_{IL} = 0.4\text{V}$, $V_{CC} = 5.25\text{V}$
I_{IH}	Input High Current			20	μA	$V_{IH} = V_{CC} = 5.25\text{V}$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_C	Input Clamp Voltage			-1.5	V	$I = -18\text{ mA}$, $V_{CC} = 4.75\text{V}$
I_{CEX1}	Output Leakage Current (All Outputs except PWR.FAIL)			1.0	mA	$V_{CC} = 5.25\text{V}$, $V_{DD} = 12.6\text{V}$
I_{CEX2}	PWR.FAIL Output Leakage Current			100	μA	$V_{OH} = V_{CC} = 5.25\text{V}$
V_{OL}	PWR.FAIL Output Low Voltage			0.4	V	$I_{OL} = 4\text{ mA}$, $V_{CC} = 4.75\text{V}$
V_{CCTH}	V_{CC} Threshold (for PWR.FAIL)		4.65		V	$V_{DD} = 12\text{V}$
V_{DDTH}	V_{DD} Threshold (for PWR.FAIL)		11.2		V	$V_{CC} = 5\text{V}$
I_{CC1}	Current from V_{CC} — Selected		30	45	mA	$CS = V_{IL}$, $V_{CC} = 5.25\text{V}$
I_{DD1}	Current from V_{DD} — Selected		20	35	mA	$CS = V_{IL}$, $V_{DD} = 5.25\text{V}$
I_{DD2}	Current from V_{DD} — Power Down		12	19	mA	$CS = V_{IH}$, $V_{DD} = 12.6\text{V}$

A.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} +5\%, -10\%$;
 $V_{DD} = 12\text{V} \pm 5\%$; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions*
t_{DON}	Propagation Delay (Turn On)	50	100	ns	
t_{DOFF}	Propagation Delay (Turn Off)	20	50	ns	
t_r	Output Current Rise Time		160	ns	See Test Setup Below
t_f	Output Current Fall Time		20	ns	See Test Setup Below
t_{DIS}	\overline{CS} Disable Time		50	ns	
t_{EN}	\overline{CS} Enable Time		500	ns	

*Note: $V_{CC} = 4.5\text{V}$ and $V_{DD} = 10.8\text{V}$ for all tests.

WAVEFORMS



Test Setup for Output Current Rise and Fall Time Measurement

CAPACITANCE*

($T_A = 25^\circ C$)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions*
C_{IN}	Input Capacitance		10	pF	

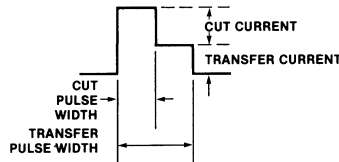
*This parameter is periodically sampled and not 100% tested. Condition of measurement is $f = 1$ MHz.

OUTPUT CURRENTS

($T_A = 0^\circ C$ to $70^\circ C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$)

Output ($V_{OUT} = 3.0V$)	Nominal Values at 50 KHz	
	Current (mA)	Pulse Width (μs)
REP.A, REP.B CUT	180	0.25
REP.A, REP.B TRANSFER	140	5.0
BOOT.REP CUT	90	0.25
BOOT.REP TRANSFER	70	5.0
GEN.A, GEN.B CUT	64	0.25
GEN.A, GEN.B TRANSFER	36	5.0
SWAP	120	28.75
BOOT.SWAP	70	See Note

Two-level pulses are defined as shown:



Note: Writing data into the bootstrap loop would require 4096 pulses of $20\mu s$ width.



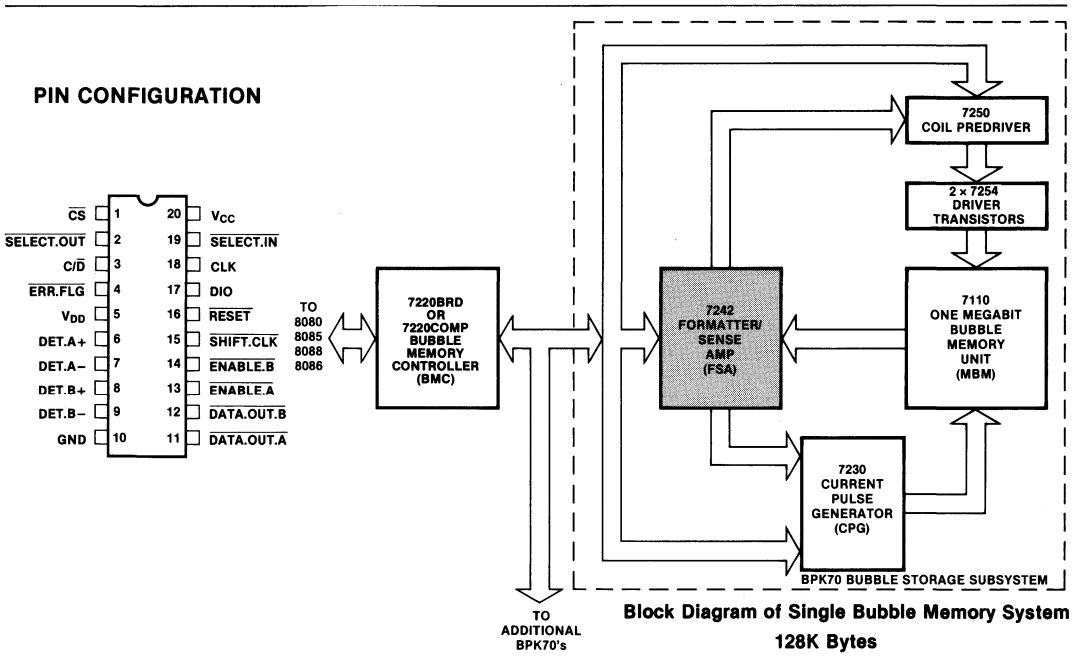
7242 DUAL FORMATTER/SENSE AMPLIFIER FOR BUBBLE MEMORIES

- Error Detection/Correction Done Automatically
 - Dual Channel
 - On-Chip Sense Amplifiers
 - Automatically Handles Redundant Loops
- FIFO Data Block Buffer
 - Daisy-Chained Selects for Multiple Bubble Memory Systems
 - MOS N-Channel Technology
 - Standard 20-Pin Dual-In-Line Package

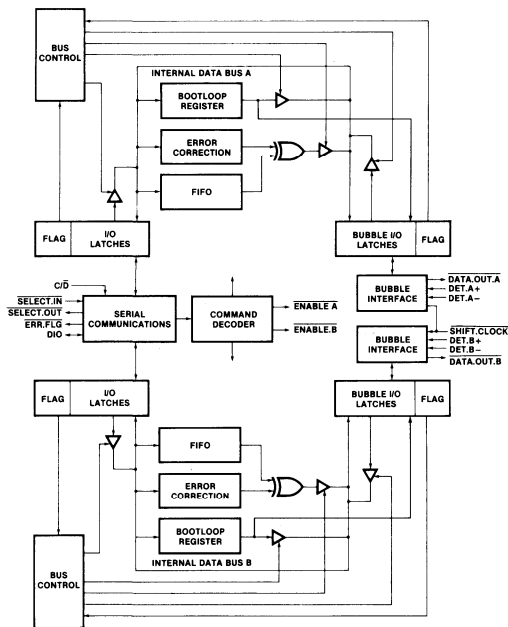
The Intel 7242 is a Dual Formatter/Sense Amplifier (FSA) designed to interface directly with Intel Magnetics Bubble Memories. The 7242 features on-chip sense amplifier for system ease of use and minimization of system part count. The 7242 also provides for automatically handling the bubble memories' redundant loops so they appear transparent to the user. In addition, complete burst error detection and correction can be done automatically by this device.

The 7242 has a full FIFO data block buffer. This device can be daisy-chained for multiple bubble memory systems. Up to eight FSA's can be controlled by one 7220 Bubble Memory Controller (BMC).

The 7242 utilizes an advanced NMOS technology to incorporate the on-chip sense amplifiers and other unique features. The device is packaged in a standard high density 20-pin dual-in-line package.



LOGIC DIAGRAM



PIN DESCRIPTION

C/D (Pin 3)

Command/Data signal. This signal shall cause the FSA to enter a receive command mode when high and to interpret the serial data line as data when low. Any previously active command will be immediately terminated by C/D.

CLK (Pin 18)

Same TTL level clock used to generate internal timing as used for 7220.

CS (Pin 1)

An active low signal used for multiplexing of FSA's. The FSA is disabled whenever CS is high (i.e., it presents a high impedance to the bus and ignores all bus activity.)

DATA.OUT.A, DATA.OUT.B (Pins 11 and 12)

Output data from the FIFO to the MBM generate circuitry. Used to write data into the bubble device (active low).

DET.A +, DET.A -, DET.B +, DET.B - (Pins 6, 7, 8, and 9)
Differential signal lines from the MBM detector.

DIO (Pin 17)

The Serial Bus data line (a bidirectional active high signal).

ENABLE.A, ENABLE.B (Pins 13 and 14)

TTL level outputs utilized as chip selects for other interface circuits. They shall be set and reset by the Command Decoder under instruction of the Controller (active low).

ERR.FLG (Pin 4)

An error flag used to interrupt the Controller to indicate that an error condition exists. It shall be an open drain active low signal.

RESET (Pin 16)

An active low signal that shall reset all flags and pointers in the FSA as well as disabling the chip as the CS signal does. The RESET pulse width must be 5 clock periods to assure the FSA is properly reset.

SELECT.IN (Pin 19)

An input utilized for time division multiplexing. An active low signal whose presence indicates that the FSA is to send or receive data from the Serial Bus during the next two clock periods.

SELECT.OUT (Pin 2)

The SELECT.IN pulse delayed by two clocks. It shall be connected to the SELECT.IN pin of the next FSA. It is delayed by two clocks because the FSA is a dual channel device. Channel A shall internally pass SELECT.IN to Channel B (delayed by one clock).

SHIFT.CLK (Pin 15)

A Controller generated clock signal that shall be used to clock data out of the bubble I/O Output Latch to the bubble module during a write operation and to cause bubble signals to be converted by the Sense Amp and clocked into the Bubble I/O Input Latch on a read.

FUNCTIONAL DESCRIPTION

The following is a brief description of each block of the 7242 FSA.

Serial Communications — The Serial Communications block handles all transfers on the Serial Bus and is shared by both channels of the FSA.

Command Decoder — The Command Decoder interprets commands by the Serial Communication logic and sets the appropriate command and enable lines. It also maintains FSA status, and generates various reset lines.

Internal Data Bus — The Internal Data Bus is the main data link between the Serial Communications block and all other data sources in each half of the FSA.

I/O Latches, Flags, and Bus Control — Each channel of the FSA has its own Internal Data Bus, on which all data transfers are made. There is a Flag and a bidirectional Latch in each "I/O Latches — Flag" block. Only one Latch is used in a given operation and the Flag tells the Bus Controller whether or not the Latch is full. The Bus Controller monitors these flags, and other control signals, to determine when each device should have access to the Internal Data Bus. When a transfer is to be made, the appropriate devices are enabled, the Bus is enabled, and the transfer takes place synchronously by virtue of a transparent State Machine Sequencer.

FIFO — The FIFO is a variable length First-In-First-Out buffer utilized to store data passing to and from the MBM module. The FIFO is logically 272 bits in length in the "no error correction" mode. It is 270 bits in the "error correction" mode, since 256 bits of data and a 14 bit error correction code must be used in this mode of operation.

The FIFO pointers are reset by hardware or software resets or each time a command to read or write is received by the Command Decoder.

If a block length other than 272 bits is used in the no error correction mode, the FIFO pointers will not return to word zero at the end of each block transfer. This is of no consequence if one is not concerned about the absolute location of data in the FIFO. Keeping in mind that the FIFO is only 272 bits physically, any block length may be used up to and including 320.

Bootstrap Loop Register — The Bootstrap Loop Register is a 160-bit register that contains information detailing the location of bad loops in the MBM module. This data will enable bubble I/O to ensure that bits are not loaded in the FIFO from bad loops, or written from the FIFO into bad loops. A logic zero (absence of a bubble) is written into bad loops.

Error Correction Logic — The Error Correction Logic contains the circuitry to implement a burst error correcting code capable of correcting any single burst error of length equal to or less than 5, anywhere in the 270-bit data stream, including the error correction code which is 14 bits in length. A Correction Enable bit may be set or reset via a special command. When reset, the entire error correction network is disabled and block length may vary from 270 bits. Error detection shall be accomplished on all data transfers (when enabled); however, correction cannot take place unless the FSA is operated in a buffered mode (i.e., an entire block is read prior to passing any data to the Controller).

Bubble I/O — The Bubble I/O consists of an integrated Sense Amplifier and an output driver. The Sense Amplifier consists of a sample-and-hold circuit and a differential, chopper stabilized comparator.

Enables — The ENABLE.A and ENABLE.B outputs are utilized as chip selects for external circuitry. To set an ENABLE line, the desired channel of the FSA must be selected and a Read or Write MBM, Set Enable Bit, Initialize, Read Corrected Data, or Internally Correct Data command is sent. Any other command sequence will reset the ENABLE lines.

COMMANDS

FSA Commands

The FSA shall receive a four-bit command word via the Serial Bus. In addition, some of the commands require additional data bits, e.g., status to be passed serially. The four bits shall be interpreted as shown in Table 1. The effects on the Status bits, Correction Enable bit, and Enable pins are summarized in Table 2.

The following is a brief description of each command available in the 7242 FSA.

No Operation — Deselects the chip and prevents further internal activity (default state for reset, unselected or unaddressed channels). Resets the FIFO and Bootloop pointers. The Enable pins (ENABLE.A and ENABLE.B) become inactive.

Software Reset — Resets all FIFO and Bootloop pointers and flags. Status flags, Error Correction Enable bit, error correction shift register, and the Enable pins become inactive.

Initialize — The chip is set to read data from the MBM Bootloop and pass it to the Controller. Resets the FIFO and Bootloop pointers and the Error Correction Logic, and disables the Bootloop register (so that it does not interfere with the data flow). The Enable pins become active in addressed channels.

Table 1. Command Code Descriptions

Code	Description	Data	
		Correction Enabled	Not Enabled
0000	No Operation	None	None
0001	(Reserved)	---	---
0010	Software Reset	None	None
0011	Initialize	MBM Bootloop	MBM Bootloop
0100	Write MBM Data	270 Bits In	Variable
0101	Read MBM Data	270 Bits Out	Variable
0110	Internally Correct Data	None	---
0111	Read Corrected Data	270 Bits Out	---
1000	Write Bootloop Register	160 Bits In	160 Bits In
1001	Read Bootloop Register	160 Bits Out	160 Bits Out
1010	(Reserved)	---	---
1011	(Reserved)	---	---
1100	Set Enable Bit	None	None
1101	Read ERR.FLG Sta'us	1 Bit Out	1 Bit Out
1110	Set Correction Enable Bit	None	None
1111	Read Status Register	8 Bits Out	8 Bits Out

Table 2. Command Function Summary

Command Description	Command Code	Data Flow (R/W)	Reset FIFO & Bootloop Pointers	Reset Status (Errors)	Reset Error Correction Logic	Enable
No Operation	0000	---	X			H
Software Reset	0010	---	X	X	X	H
Initialize	0011	R	X	X	X	L
Write MBM Data	0100	W	X		X	L
Read MBM Data	0101	R	X		X	L
Internally Correct Data	0110	---	X			L
Read Corrected Data	0111	R	X			L
Write Bootloop Register	1000	W	X			H
Read Bootloop Register	1001	R	X			H
Set Enable Bit	1100	---	X			L
Read ERR.FLG Status	1101	R				H
Set Error Correction Enable Bit	1110	---	X			H
Read Status Register	1111	R		X		H

Write MBM Data — Data input by the Controller is written into the good loops in use in the MBM (under control of the Bootloop register) each time a **SHIFT.CLK** is received. It also activates the Enable pins and resets the FIFO and Bootloop pointers. If the Correction Enable bit is set, the FSA computes the correction code and appends it to the data stream to be stored in the MBM (last 14 of 270 bits).

Read MBM Data — This command activates the **ENABLE** pins and resets the FIFO and Bootloop pointers independent of the state of the Correction Enable bit. If the Correction Enable bit is reset, data from the MBM, of block length dictated by 2 times the number of logic “1s” in the Bootloop register, is sensed and screened by the FSA Sense Amp and Bootloop register, and stored in the FIFO. As soon as one bit is guaranteed in the FIFO, simultaneous reading from the FIFO may be done by the Controller. The FIFO need not be emptied after each page is read, but one must insure that more than 272 bits of FIFO are not needed at any time during the transfer.

If the Correction Enable is set, data must be read in a buffered mode. First, a full block of data is read from the MBM. At that point the FIFO contains 270 bits of data. If an error is detected by the Error Correction network, the FSA raises the **UNCORR.ERR** and **CORR.ERR** flags which generate an interrupt to the controller. If no error is detected, the 270 bits of data may be read from the FIFO while simultaneously reading and checking the next block of data from the MBM. When an error is detected the Controller may respond to the interrupt in one of three ways.

1. Ignore it and try again (must make sure to reset the Error Correction shift register before a retry).
2. Send a Read Corrected Data command to the FSA. This command will correct the data stream (if possible) and interrupt the Controller when the block has been read. At this time the Controller can send a

Read Status command to see if the error was correctable (**CORR.ERR**) or uncorrectable (**UNCORR.ERR**).

3. Send an Internally Correct Data command to the FSA. The FSA corrects the data without transferring it to the Controller. When finished, the FSA interrupts the Controller. At this point it can be determined whether or not the error is correctable. If so, a Read Corrected Data command may be sent to read the good data.

Internally Correct Data — Internally cycles the data through the error correction network and returns status as to whether or not the data is correctable.

Requires approximately 1400 clock cycles to complete. **ERR.FLG** will be inactive during internal cycling, but will return active at its completion. Also activates the **ENABLE** pins and resets the FIFO and Bootloop pointers.

Read Corrected Data — Cycles data through the error correction network with each Controller read (**SELECT.IN** at the FSA). At the end of 270 reads, status is available to indicate whether or not the data was successfully corrected. **ERR.FLG** acts as in Internally Correct Data. This command is required to read data corrected internally as well, but has no effect on the data read if it was successfully corrected. Activates the **ENABLE** pins and resets the FIFO and Bootloop pointers.

Write Bootloop Register — Contents of the FSA's Bootloop register are written with 160 bits from the Controller. The Controller must read the MBM Bootloop first, to determine which loops are good. The number of good bits in the 160-bit register is 135 if correction is used, and variable up to 160 if operating in the no correction mode. **ENABLE** pins become inactive and the FIFO and Bootloop pointers are reset.

Read Bootloop Register — As above except that data is read from the FSA Bootloop to the Controller.

Set Enable Bit — **ENABLE** pins become active for addressed channels, inactive for unaddressed channels. Also resets the FIFO and Bootloop pointers.

Read ERR.FLG Status — Reads the composite error status for addressed channels of the FSA. (The composite status is the logic OR of CORR.ERR, UNCORR.ERR and TIMER.R. The ERR.FLG pin is the logic NOR of both channels' composite error status: ERR.FLG.A and ERR.FLG.B.) ENABLE pins become inactive.

Set Error Correction Enable Bit — Enables the Error Correction Logic in addressed FSAs and disables it in unaddressed FSAs. ENABLE pins become inactive and FIFO and Bootloop pointers are reset. Furthermore, when this enable is set, the corresponding FIFO becomes a 270-bit FIFO (logically) instead of a 272-bit FIFO as in the no correction mode.

Read Status Register — The 8-bit Status Word for the addressed FSA is output to the Controller. Only one FSA channel can be addressed at a time, or bus contention may result. ENABLE pins become inactive and error flags in the addressed FSA channel are reset.

SERIAL INTERFACE

Command Sequence — The FSA communicates with the Controller via a Serial Interface. The Controller/FSA Interface contains the following signals:

1. CLK
2. SELECT.IN (Formatter)
3. SELECT.OUT (Formatter)
4. SYNC (Controller)
5. DIO
6. C/D
7. SHIFT.CLK
8. ERR.FLG

Commands from the Controller to the FSA shall take place in the following format (see Figure 1).

1. Controller raises C/D flag indicating that a command is coming, and simultaneously outputs a SYNC pulse. This SYNC pulse is shifted down the FSA chain in shift register fashion via the FSA SELECT.IN/SELECT.OUT lines.
2. Controller outputs a serial data stream on the DIO line beginning in the clock period following SYNC. Each bit in the stream corresponds to an address bit for a particular FSA (up to 16 channels). Each FSA, upon receiving SELECT.IN, will look for the presence or absence of a logic one on DIO in the clock period following receipt of SELECT.IN. (A logic one indicates that the FSA shall accept the command.)
3. Twenty clock periods after the first SYNC, the Controller sends C/D low followed by a four-bit command on the DIO line.
4. If the command is a Read Status command (1111), the addressed FSA returns 8 bits of Status starting 4 clock periods after the last command bit is received. Note that the Status is returned during this period for any FSA position. Therefore only one FSA channel should be addressed at a time to avoid contention.
5. If the command requires further data (see section on FSA Commands), more SYNC pulses are sent by the Controller. This will occur at integral multiples of 80 or 20 clock periods starting no sooner than 40 clocks after the first command SYNC pulse. Some number of SYNC periods may pass before the second SYNC to allow the FSA to set itself up and get data ready for the Controller. There are several possibilities:
 - a. For the Read ERR.FLG Status command the second SYNC can occur 40 clocks after the first SYNC. This SYNC (or SELECT.IN) causes each addressed FSA to send the appropriate Status information. No further SYNCs (without C/D high) should be sent.

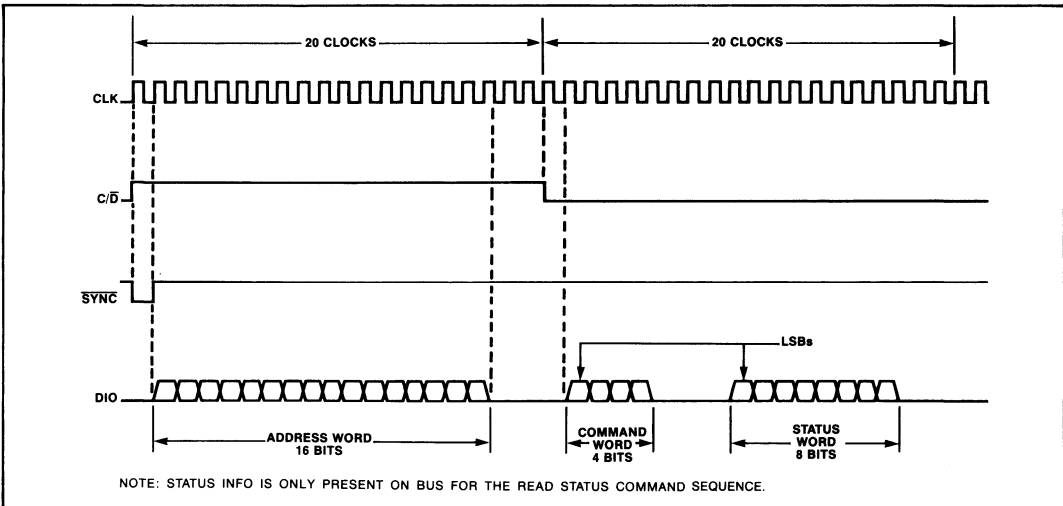


Figure 1. Command Sequences

- b. For the Read MBM Data (or Initialize) command the second SYNC must wait the appropriate number of SHIFT.CLOCKS to assure that valid data is available in the FIFO.
After this wait, each addressed FSA channel sends one bit of data on the DIO line for each SYNC (or SELECT.IN) pulse.
 - c. For the Read Bootloop Register command, the second SYNC can occur 60 clock cycles after the first SYNC. The data transfer then proceeds as in b. above.
 - d. For the Write MBM Data or Write Bootloop commands, the DIO line is used to transfer data to the FSA on successive SYNC pulses. The first data bit can be transferred by a second SYNC pulse, 40 clock cycles after the first SYNC. (However, data to the MBM will not be available at the Dataout pins until 40 clock cycles after the SYNC which transferred it.) Each transfer to the addressed FSA will be initiated by a SYNC (or SELECT.IN).
6. SYNC (SELECT.IN) precedes the data it transfers by 1 clock cycle. Data transfers to or from the FSA's FIFO must contain the proper number of SYNCs (externally counted) or a timing error may occur (TIMERR flag will be set, causing an interrupt to the Controller).

Data Sequences — Bubble data shall be passed between the Controller and FSAs in the following fashion (see Figure 2).

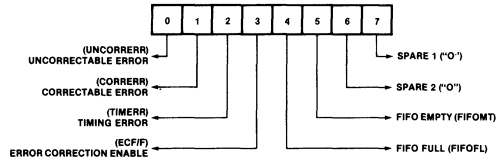
1. Controller outputs a SYNC pulse.

2. Each FSA then outputs (inputs) a single bit on DIO after SYNC (SELECT.IN) has been clocked into its control section. Only previously enabled FSAs output (input) data and the Controller must know when to input (output) data bits.
3. After 80 or 20 clocks, another SYNC pulse is output and the sequence repeats until all data has been transferred.

Error Conditions — Each FSA shall upon detection of an error set a Status bit and pull down ERR.FLG. This signal can be asynchronous to SYNC. Error Status bits shall be:

1. Correctable Error
2. Uncorrectable Error
3. Timing Error

The Status Word that shall be passed to the Controller after receipt of a Read Status command shall be in the following format:



NOTE: ERROR FLAGS SHALL BE RESET UPON BEING READ BY THE CONTROLLER OR BY A SOFTWARE RESET OR INITIALIZE.

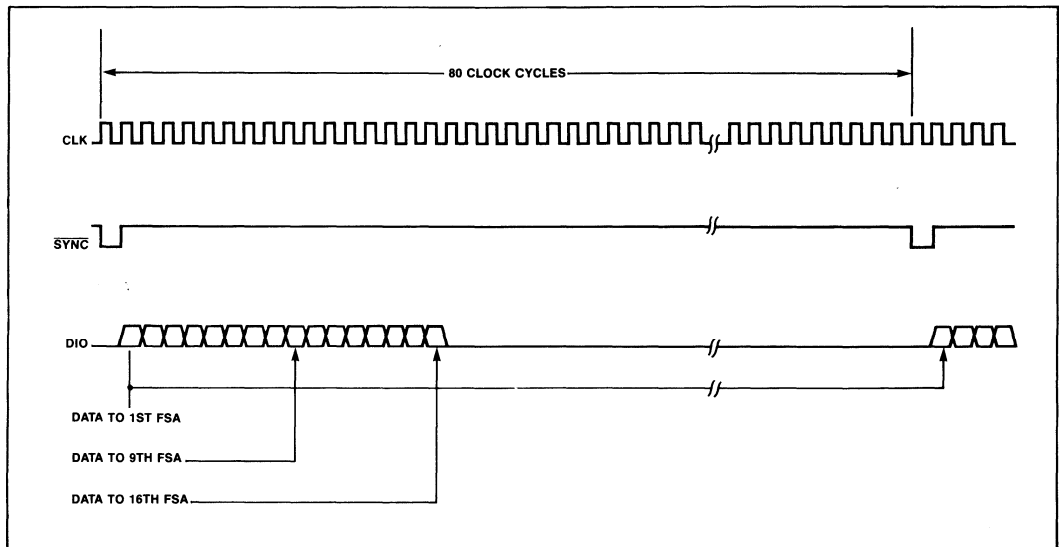


Figure 2. Data Sequences

BUBBLE INTERFACE

Bubble Interface — Each Bubble Interface shall consist of a DATAOUT signal and a pair of differential inputs from the MBM detector bridge.

Read Timing — The timing for reading a bit from the memory shall be as follows:

1. Controller outputs a $\overline{\text{SHIFT.CLK}}$. FSA samples bubble signal during $\overline{\text{SHIFT.CLK}}$ and holds signal after trailing edge.
2. Trailing edge of $\overline{\text{SHIFT.CLK}}$ initiates signal conversion timing.
3. Data is latched at end of conversion period in the Bubble Input latch, and will subsequently be loaded into the FIFO.

Write Timing — The timing for writing a bit from the FIFO shall be as follows:

1. Controller lowers $\overline{\text{SHIFT.CLK}}$.
2. Data is gated out of FSA by $\overline{\text{SHIFT.CLK}}$.
3. Controller outputs a generate pulse (to external logic; not to FSA).
4. Controller raises $\overline{\text{SHIFT.CLK}}$. The DATA.OUTPUT pin is forced high.
5. FIFO and Bootloop register are incremented after the leading edge of $\overline{\text{SHIFT.CLK}}$.

System Timing — The SYNC pulse (which denotes the beginning of a data transfer from Controller to Formatter or vice-versa) shall be synchronous with the beginning of a bubble memory field rotation. Due to timing constraints in the FSA, the following statements hold:

1. Data read from the bubble memory into the FSA shall not be available to the Controller until 40 clock cycles after $\overline{\text{SHIFT.CLK}}$.
2. Data cannot be written to the bubble memory until 40 clock cycles after SYNC.

FSA ERROR CORRECTION

Error Correction — The error correction logic consists of a burst error correcting Fire code capable of correcting 5 or fewer bits in a single burst; the number of check bits is 14.* Error correction/detection shall take place on each 256-bit data block. The FSA shall set low ERR.FLG each time a correctable or uncorrectable error is detected. ERR.FLG shall be set high upon being read by the Controller or by a software reset being issued. The polynomial implemented is given below:

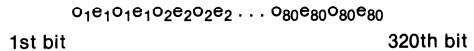
$$G(X) = 1 + X^2 + X^5 + X^9 + X^{11} + X^{14}$$

DATA FORMAT

Data Format—Data into a single FSA channel from the bubble memory shall be in the format described below. The two channels of the bubble are represented identically. The following definitions apply:

- o_n = data from odd half of bubble device, loop n
- e_n = data from even half of bubble device, loop n

Data Block Format —



When using correction, the first 270 good bits will be used; the last 14 of these are to be used for the error correcting code. The remaining 50 bits must be masked as “bad” bits in the FSA Bootloop register.

When operating without correction, any number of bits may be used by loading the Bootloop register appropriately. The preferred number is 272 bits, however.

*See “Error-Correcting Codes” by W.W. Peterson and E. J. Weldon, Jr., pp. 366–370, M.I.T. Press, 1972.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages and V _{CC} Supply Voltage	-0.5V to +7V
V _{DD} Supply Voltage	-0.5V to +14V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5.0V +5%, -10%; V_{DD} = 12V ±5%)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V _{IL}	Input Low Voltage	-0.5		0.8	V	
V _{IH}	Input High Voltage	2.0		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage (All Outputs Except SELECT.OUT)			0.45	V	I _{OL} = 3.2 mA
V _{OLSO}	Output Low Voltage (SELECT.OUT)			0.45	V	I _{OL} = 1.6 mA
V _{OH}	Output High Voltage (All Outputs Except SELECT.OUT)	2.4			V	I _{OH} = 400 μA
V _{OHSO}	Output High Voltage (SELECT.OUT)	2.4			V	I _{OH} = 200 μA
V _{THR}	Detector Threshold	2.0		3.0	mV	V _{DD} = 12.0V
I _{IL}	Input Leakage Current			10	μA	0 ≤ V _{IN} ≤ V _{CC}
I _{OFL}	Output Float Leakage			10	μA	0.45 ≤ V _{OUT} ≤ V _{CC}
I _{CC}	Power Supply Current from V _{CC}			120	mA	
I _{DD}	Power Supply Current from V _{DD}			30	mA	

A.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} \pm 5\%$, -10% ;
 $V_{DD} = 12\text{V} \pm 5\%$; $C_L = 120\text{ pF}$; unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_p	Clock Period	240	500	ns	
t_ϕ	Clock Phase Width	$0.4 t_p$	$0.6 t_p$		
t_r, t_f	Clock Rise and Fall Time		30	ns	
t_{SIC}	$\overline{\text{SELECT.IN}}$ Setup Time to CLK	50		ns	
t_{CDC}	$\text{C}/\overline{\text{D}}$ Setup Time to CLK	50		ns	
t_{CYC}	$\overline{\text{SELECT.IN}}$ or SHIFT.CLK Cycle Time	$20 t_p$			
t_{DC}	DIO Setup Time to Clock (Read Mode)	50		ns	
t_{CSC}	$\overline{\text{CS}}$ Setup Time to CLK	100		ns	
t_{RIC}	$\overline{\text{RESET.IN}}$ Setup Time to CLK	100		ns	
t_{IH}	Control Input Hold Time for $\text{C}/\overline{\text{D}}$, $\overline{\text{SELECT.IN}}$ and DIO	20		ns	
t_{CSOL}	CLK to $\overline{\text{SELECT.OUT}}$ Leading Edge Delay		100	ns	$C_L = 50\text{ pF}$
t_{CSOT}	CLK to $\overline{\text{SELECT.OUT}}$ Trailing Edge Delay		100	ns	$C_L = 50\text{ pF}$
t_{CDV}	CLK to DIO Valid Delay*		100	ns	
t_{CDH}	CLK to DIO Hold Time*	0		ns	
t_{CDE}	CLK to DIO Enabled from Float*		100	ns	
t_{SIDE}	$\overline{\text{SELECT.IN}}$ Trailing Edge to DIO Enabled from Float*		70	ns	
t_{CDF}	CLK to DIO Entering Float*		100	ns	
t_{SCDO}	$\overline{\text{SHIFT.CLK}}$ to DATAOUT Delay*		200	ns	
t_{SCWR}	$\overline{\text{SHIFT.CLK}}$ Width (Read)	$4 t_p$	$t_{CYC} - 11 t_p$		
t_{SCWW}	$\overline{\text{SHIFT.CLK}}$ Width (Write)	t_p	$t_{CYC} - 2 t_p$		

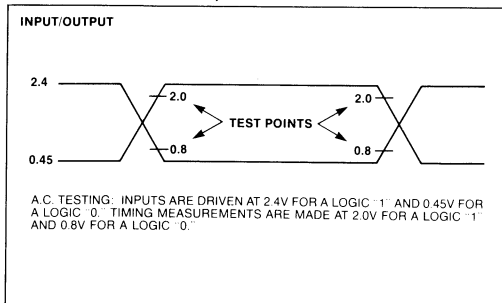
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 0\text{V}$, $f = 1\text{ MHz}$)

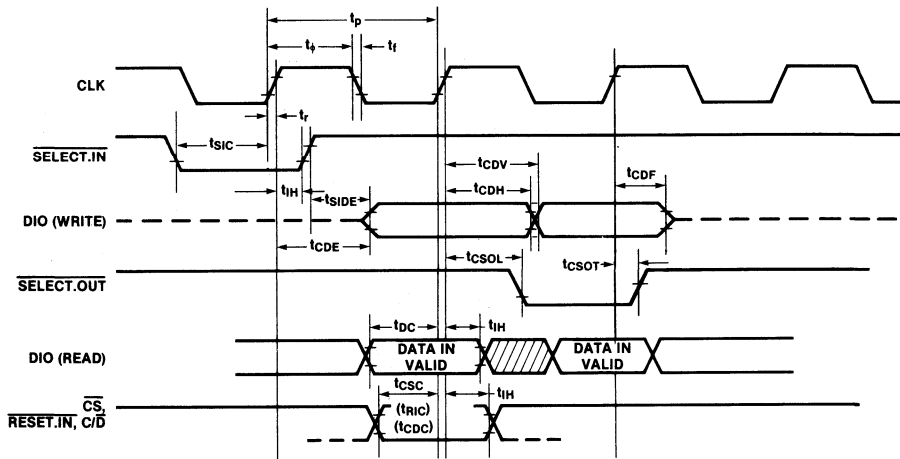
Symbol	Parameter	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	
C_{DIO}	DIO Capacitance		10	pF	

*DIO Write Mode.

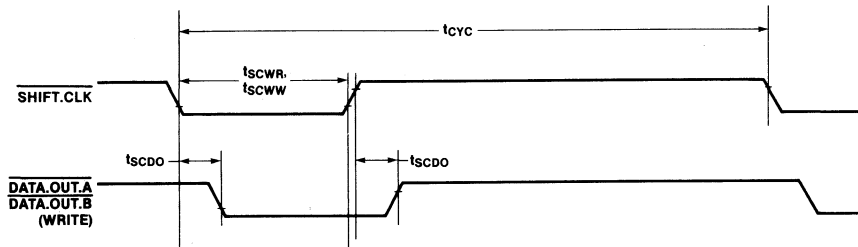
A.C. TESTING INPUT, OUTPUT WAVEFORM



DIO INTERFACE TIMING



BUBBLE DATA INTERFACE TIMING





7250 COIL PRE-DRIVER FOR BUBBLE MEMORIES

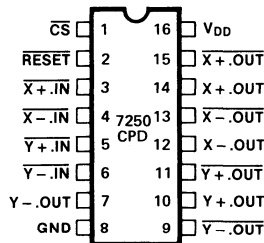
- Very Low Power
- Power Fail Reset for Maximum Protection of Bubble Memory
- TTL Compatible Inputs
- Only One Power Supply Required, + 12V
- CMOS Technology
- Standard 16-Pin Dual In-Line Package

The Intel 7250 is a low power Coil Pre-Driver (CPD) for use with Intel Magnetics Bubble Memories. The 7250 is controlled by the Intel 7220 Bubble Memory Controller (BMC) and directly drives either Quad VMOS transistor packs or Quad Bipolar transistor packs which are connected to the coils of the bubble memory.

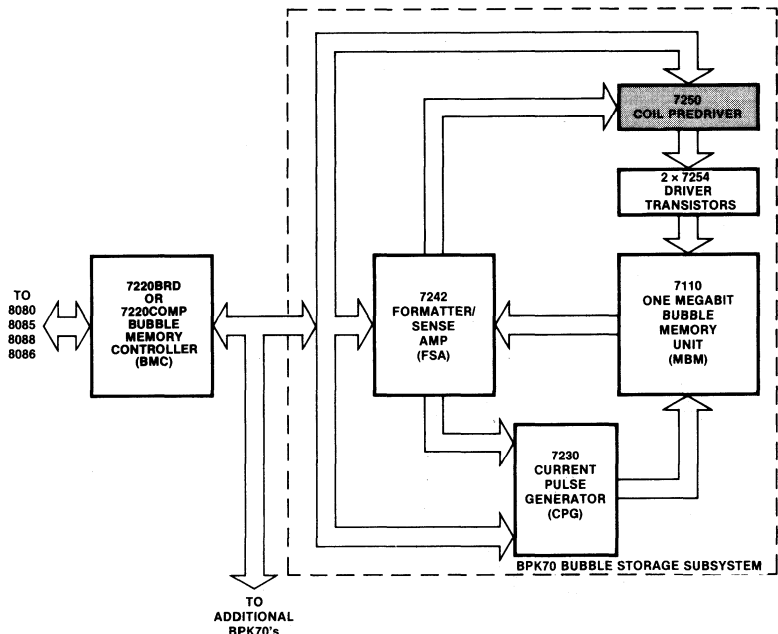
The 7250 is a high voltage, high current driver constructed using CMOS technology. The device has TTL compatible inputs and the outputs are designed to drive either low on-resistance VMOS transistors or bipolar transistors.

The 7250 is in a standard 16-pin dual in-line package.

PIN CONFIGURATION



BLOCK DIAGRAM



Block Diagram of Single Bubble Memory System — 128K Bytes

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . - 20°C to + 80°C
 Storage Temperature - 65°C to + 150°C
 Voltage on Any Pin with
 Respect to Ground - 0.5 to $V_{DD} + 0.5V$
 Supply Voltage, V_{DD} - 0.5 to + 14V
 Output Current 250 mA
 (One Output @ 100% Duty Cycle)

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

($T_A = 0^\circ C$ to $+70^\circ C$; $V_{DD} = 12V \pm 5\%$, -10% ; unless otherwise specified)

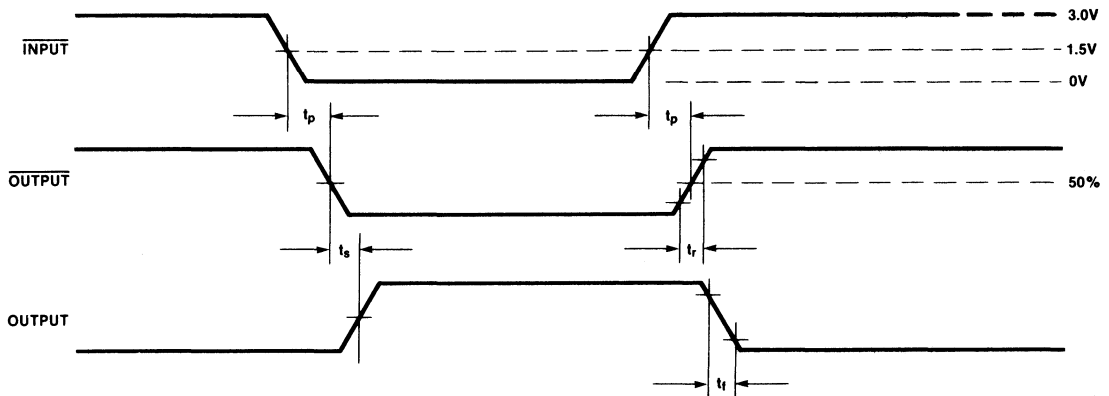
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
$ I_{IN} $	Input Current			10	μA	$V_I = 0.8V$
V_{IL}	Low Level Input Voltage			0.8	V	
V_{IH}	High Level Input Voltage	2.2			V	
V_{OL1}	Output Low Voltage			2.0	V	$I_{OL} = 200\text{ mA}$
V_{OL2}	Output Low Voltage			0.2	V	$I_{OL} = 10\text{ mA}$
V_{OH1}	Output High Voltage	$V_{DD}-2$			V	$I_{OH} = -200\text{ mA}$
V_{OH2}	Output High Voltage	$V_{DD}-0.2$			V	$I_{OH} = -10\text{ mA}$
I_{OL}	Output Sink Current	200			mA	$V_{OL} = 2.0V$, 30% Duty Cycle
$ I_{OH} $	Output Source Current	200			mA	$V_{OH} = V_{DD}-2.0V$, 30% Duty Cycle
I_{DD0}	Supply Current			4.5	mA	Chip Deselected: $\overline{CS} = V_{IH}$, $V_{DD} = 12.6V$
I_{DD1}	Supply Current			75	mA	$f = 100\text{ kHz}$, $V_{DD} = 12.6V$, Outputs Unloaded
I_{DD2}	Supply Current			90	mA	$f = 200\text{ kHz}$, $V_{DD} = 12.6V$ Outputs Unloaded

A.C. CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 12\text{V} \pm 5\%$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{p1}	Propagation Delay from $\overline{X+.IN}$, $\overline{X-.IN}$, $Y+.IN$, $\overline{Y-.IN}$			100	ns	500 pF Load
t_{p2}	Propagation Delay from \overline{CS} or \overline{RESET}			150	ns	500 pF Load
t_r	Rise Time (10% to 90%)			45	ns	500 pF Load
t_f	Fall Time (90% to 10%)			45	ns	500 pF Load
t_s	Skew Between an Output and its Complement			20	ns	

A.C. TEST CONDITIONS



CAPACITANCE* ($T_A = 25^\circ\text{C}$, $V_{DD} = 0\text{V}$, $V_{BIAS} = 2\text{V}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	

*This parameter is periodically sampled and is not 100% tested.

PIN DESCRIPTION

\overline{CS} (Pin 1)

Chip select. It is active low. When high chip is deselected and I_{DD} is significantly reduced.

RESET (Pin 2)

Active low input from RESET.OUT of 7220 Controller forces 7250 outputs inactive so that bubble memory is protected in the event of power supply failure.

$\overline{X+IN}$, $\overline{X-IN}$ (Pins 3, 4)

Active low inputs from controller which turn on the high current X outputs.

$\overline{X-.OUT}$, $\overline{X+.OUT}$, $X+.OUT$, $X-.OUT$ (Pins 12-15)

High current outputs and their complements for driving the gates of the 7254 VMOS quad transistors which in turn drive the X coils of the bubble memory.

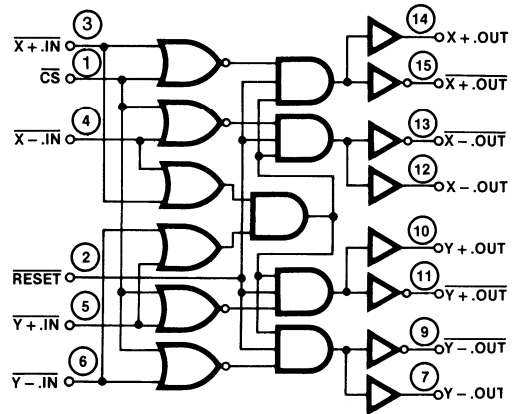
$\overline{Y+.IN}$, $\overline{Y-.IN}$ (Pins 5, 6)

Active low inputs from controller which turn on the high current Y outputs.

$\overline{Y-.OUT}$, $Y+.OUT$, $Y+.OUT$, $Y-.OUT$ (Pins 9-11 and 7)

High current outputs and their complements for driving the gates of the 7254 VMOS quad transistors which in turn drive the Y coils of the bubble memory.

LOGIC DIAGRAM

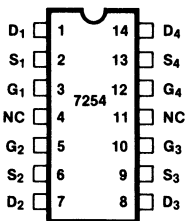


7254 QUAD VMOS DRIVE TRANSISTORS FOR BUBBLE MEMORIES

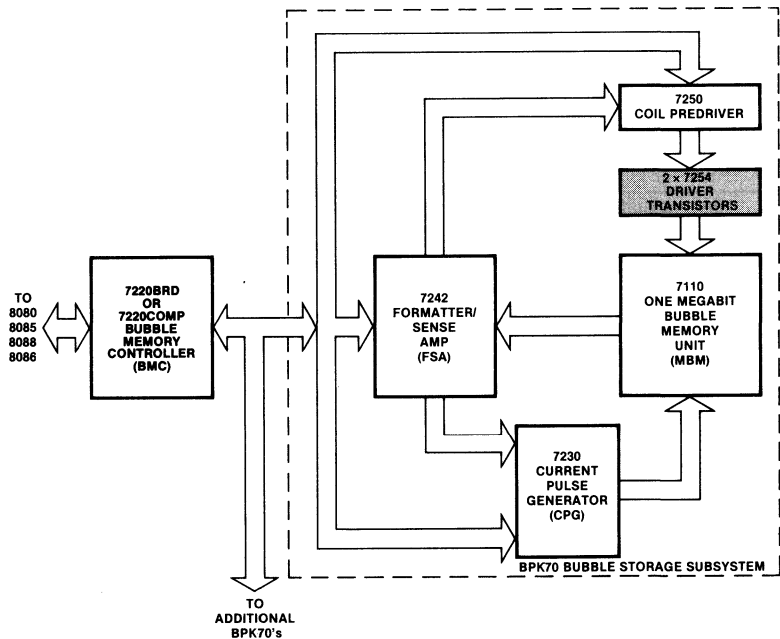
- Designed to Drive X and Y Coils of 7110 Bubble Memories
- No Bias Currents Required
- Fast Turn-on and Turn-off: 30 ns Maximum
- Built-in Diode Commutates Coil Current When Transistor is Turned Off
- Operates from V_{DD} Only
- VMOS FET Technology
- N-Channel and P-Channel Transistors in the Same Package
- Standard 14-Pin Dual-In-Line Package

The 7254 is a quad transistor pack designed to drive the X and Y coils of Intel Magnetics Bubble Memories. Two 7254 packages are required for each bubble memory device. Each 7254 package would drive either the X or Y coil as shown under "circuit diagram." This recommended connection circuit takes into account the fact the Q1/Q2 and Q3/Q4 are tested as a pair for "On" resistance value to assure optimal bubble performance.

PIN CONFIGURATION



BLOCK DIAGRAM



Block Diagram of Single Bubble Memory System — 128K Bytes

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias -20° to +85°C
 Storage Temperature -40° to +150°C
 Drain Voltage (with respect to Gate or Source) 30V
 Continuous Drain Current 2A
 Peak Drain Current 3A
 Power Dissipation (T_A = 80°C) 1.05W
 Power Dissipation (T_A = 25°C) 1.75W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

All Limits Apply for N- and P-Channel transistors, T_A = 0 to 70°C unless otherwise noted.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
BV _{DSS}	Drain-Source Breakdown Voltage	20			V	V _{GS} = 0, I _D = 10 μA
V _{GS(th)}	Gate-Source Threshold Voltage	0.8			V	V _{GS} = V _{DS} , I _D = 1 mA
I _{GSS}	Gate Leakage Current			10	μA	V _{GS} = 12V, V _{DS} = 0, T _A = 85°C
I _{DSS}	Drain Leakage Current			500	μA	V _{GS} = 0, V _{DS} = 20V, T _A = 85°C
R _{DS}	On-Resistance for sum of Q1+Q2, Q3+Q4 (Note 1)	2.0	2.5	3.0	Ω	V _{GS} = 11.4V, I _D = 1A, T _A = 25°C
V _{F1}	Parasitic Diode Forward Voltage (Note 1)			.75	V	V _{GS} = 0V, I _D = 50mA, T _A = 25°C
V _{F2}	Parasitic Diode Forward Voltage (Note 1)			1.20	V	V _{GS} = 0V, I _D = 1000mA, T _A = 25°C

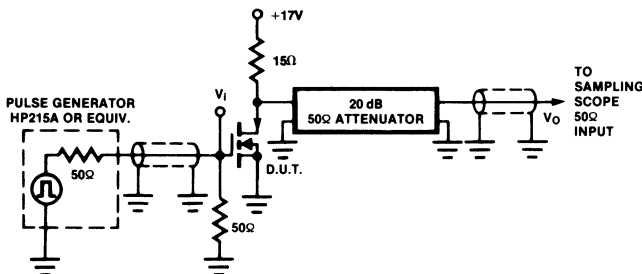
Note: 1. Pulse test — 80 μs pulse, 1% duty cycle, r_{DS} increase 0.6%/°C.

A.C. CHARACTERISTICS

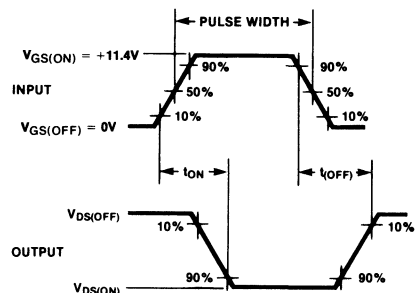
T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t _{ON(N)}	N-Channel Turn-On Time			20	ns	See Switching Time Test Circuit and Waveforms below
t _{ON(P)}	P-Channel Turn-On Time			30	ns	
t _{OFF(N)}	N-Channel Turn-Off Time			20	ns	
t _{OFF(P)}	P-Channel Turn-Off Time			30	ns	

SWITCHING TIME TEST CIRCUIT



SWITCHING TIME TEST WAVEFORMS

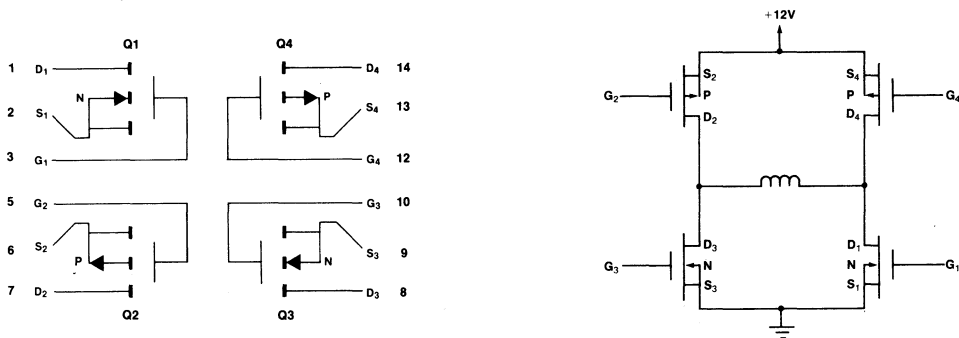


Capacitance

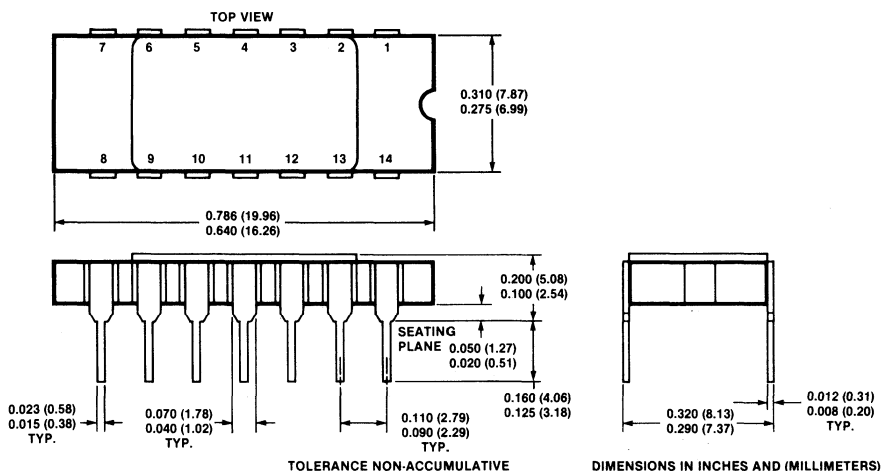
$T_A = 25^\circ\text{C}$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}(N)$	N-Channel Input Capacitance			175	pF	$V_{GS} = 0, V_{DS} = 12V, f = 1\text{ MHz}$
$C_{iss}(P)$	P-Channel Input Capacitance			190	pF	$V_{GS} = 0, V_{DS} = 12V, f = 1\text{ MHz}$

CIRCUIT DIAGRAM



PACKAGING INFORMATION



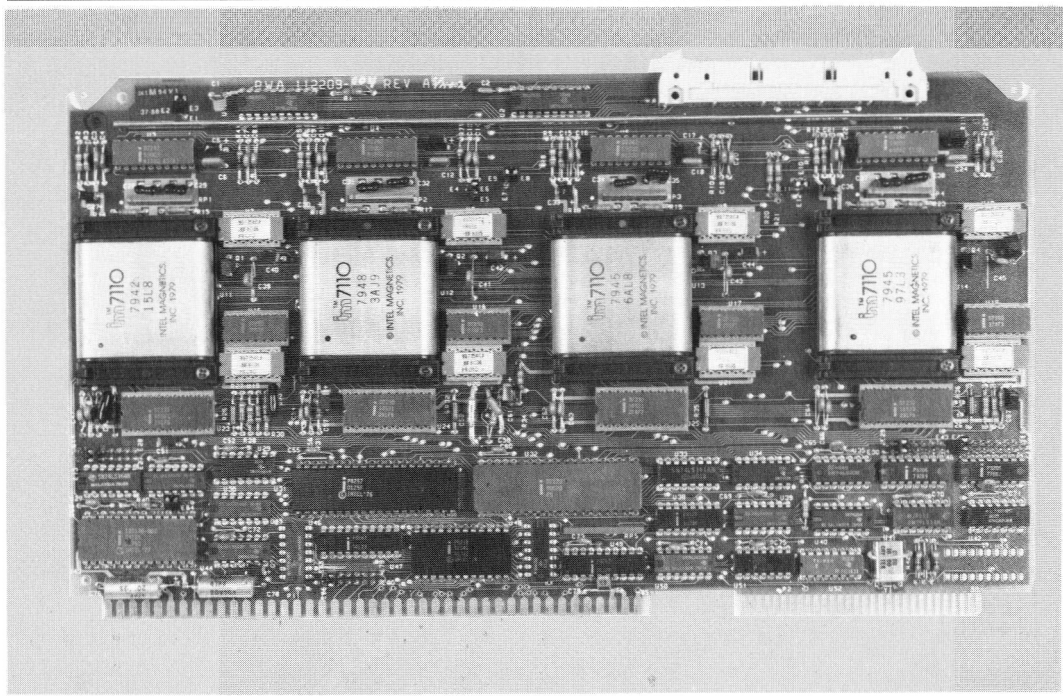
iSBC 254™ BUBBLE MEMORY BOARD

- Capacity up to 512K Bytes of Bubble Memory Storage
- Automatic Error Correction
- Operates from Standard +5V and +12V Power Supplies
- High-Density Storage
- DMA Capability
- Non-Volatile Storage
- Average Access Time of 48ms
- Burst Data Rate up to 50K Bytes per Second
- Software Compatible with the iRMX™ Operating System
- Powerfail Data Protection
- Low Power Consumption (32 Watts per ½ Megabyte)

The iSBC 254 board is a completely assembled and tested non-volatile memory utilizing the Intel 7110 one-megabit bubble memory. This board is offered with one, two, or four 7110 bubble memories, thus yielding capacities of 128K, 256K, or 512K bytes.

Software support is provided under both iRMX/80 and iRMX/86 operating systems, and DMA capability provides the user with considerable flexibility and control. Because of the solid-state nature of this technology, the iSBC 254 board is ideally suited for applications in harsh or rugged environments.

The iSBC 254 board is compatible with 16-bit addressing for 8-bit processors and with 20-bit addressing for 16-bit processors.



OPERATIONAL DESCRIPTION

Three distinct modes of operation relate to the transfer of data. Each is briefly described below.

Data Transfer

In DMA (Direct Memory Access) Mode, the iSBC 254 board utilizes the Intel 8257 DMA Controller, in conjunction with the 7220 Bubble Memory Controller, to perform three distinct types of DMA operation: DMA Read, DMA Write, and DMA Verify. In a DMA Read operation, data is transferred from memory to the FIFO (first-in/first-out RAM) of the 7220 BMC (Bubble Memory Controller). In a DMA Write operation, data is transferred from the 7220 BMC FIFO to memory. In a DMA Verify operation, the iSBC 254 board gains control of the bus, but no actual transfer of data takes place. DMA Read and DMA Write operations are used for high-speed data transfers involving bus-accessible memory; DMA Verify operations are typically used to maintain control of the system bus while verification tasks, such as checking newly acquired data, are being performed.

In Polled Mode, the CPU periodically checks the Status Register of the 7220 BMC. The Status Register can indicate a variety of conditions, one of which is that the BMC FIFO is ready to receive data or that the FIFO contains data to be read.

In DRQ (Data Request) Mode, when the FIFO of the 7220 BMC is half empty (during a write operation) or half full (during a read operation), the DRQ pin becomes active and an interrupt is issued, signalling that data may be written (bus to iSBC 254 board) or read (iSBC 254 board to bus).

Two distinct modes of operation relate to monitoring the bubble memory board status (via the 7220 Bubble Memory Controller). Each is briefly described below.

Status Monitoring Modes

In Interrupt Mode, a change in the 7220 BMC Status Register will cause an interrupt to occur, and the host processor will then look at that register to see what change has occurred. Any of the following may be

indicated: the BMC sequencer is busy; an operation has been completed; an operation has failed; a timing error has occurred; and/or a correctable, uncorrectable, or parity error has occurred.

In Polled Mode, as described above under Data Transfer, the CPU periodically checks the Status Register of the 7220 BMC. The Status Register can indicate a variety of conditions: that the BMC Sequencer is busy; that an operation is complete; that an operation has failed; that a timing error has occurred; that a correctable, uncorrectable, or parity error has occurred; or, in terms of data transfer, that the BMC FIFO is ready to receive data or that the FIFO contains data to be read.

SOFTWARE DESCRIPTION

The iSBC 254 board can run under either the iRMX/80 or the iRMX/86 operating system.

Under the iRMX/80 operating system, the Bubble Manager (BMGR), a software task that runs with the iRMX/80 operating system, keeps track of free or available space on the Magnetic Bubble Memory. Another task, Bubble I/O (BUBIO), controls all iSBC 254 board operations. Bubble I/O can run with or without the Bubble Manager.

Under the iRMX/86 operating system, the iSBC 254 board is supported as an integral part of the I/O system software, which is part of the iRMX/86 operating system. (The iRMX/86 operating system device driver for the iSBC 254 board is linked with the I/O system software, which is in turn linked with the iRMX/86 operating system.) Because the iRMX/86 operating system provides convenient codes for performing operations, because all devices "look" the same when running under this operating system, and because of a variety of built-in features, the iRMX/86 operating system provides great flexibility.

Software programs on both single- and double-density diskettes are provided with the iSBC 254 board. EX-254 is a set of programs that demonstrates how to use the various iSBC 254 board software commands.

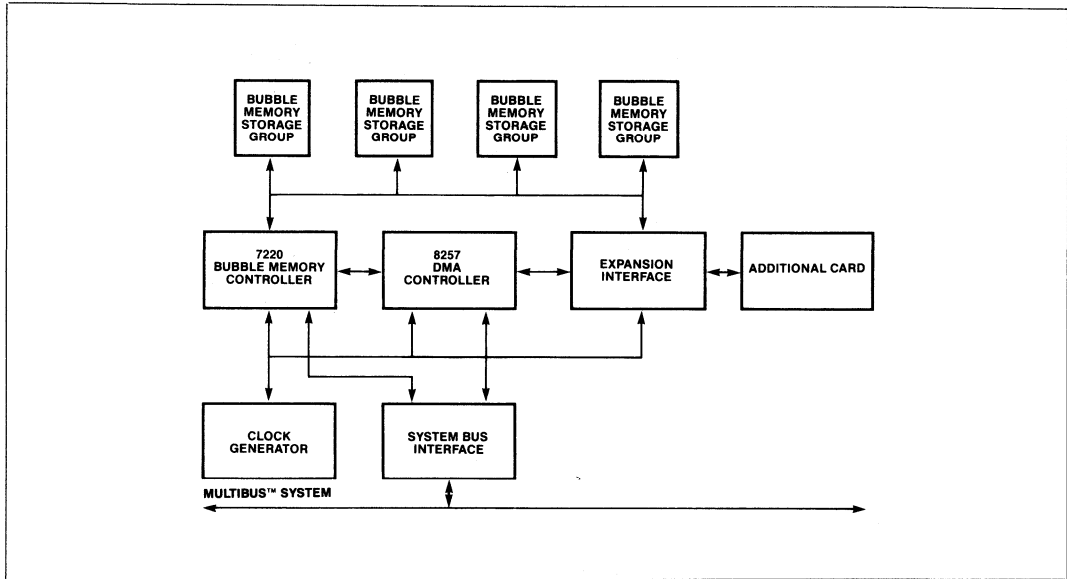


Figure 1. iSBC 254™ Board, Block Diagram

SPECIFICATIONS

Memory Size

128K, 256K, or 512K bytes

Interface

All address, data, and control signals are TTL-compatible and Intel MULTIBUS system compatible.

Electrical Characteristics

D.C. Power

- +5 volts D.C. ±5%, 3.0A (max.)
- +12 volts D.C. ±5%, 1.4A (max.)

Performance

- Rotating Field Rate: 50KHz
- Maximum Data Rate: 50K bytes/second
- Average Access Time: 48ms

Connector

86-pin double-sided PC edge connector with 0.40 cm (0.156 in.) contact centers.
 Mating Connector: Control Data VFB01E43D0A1 or Viking 2VH43/1ANE5.

Physical Characteristics

- Length: 30.48 cm (12 in.)
- Height: 17.15 cm (6.75 in.)
- Depth: 1.57 cm (0.62 in.)

Note: Because of its depth, the iSBC 254 board requires two card slots.

Environment

Board Operating Temperature: 0–55°C

Equipment Supplied

- iSBC 254 Bubble Memory Board
- iSBC 254 Operation Manual
- iSBC 254 Software (single- and double-density diskettes)



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